Customer Training Workshop
Traveo™ II Body Entry
SRAM Interface

Q4 2020

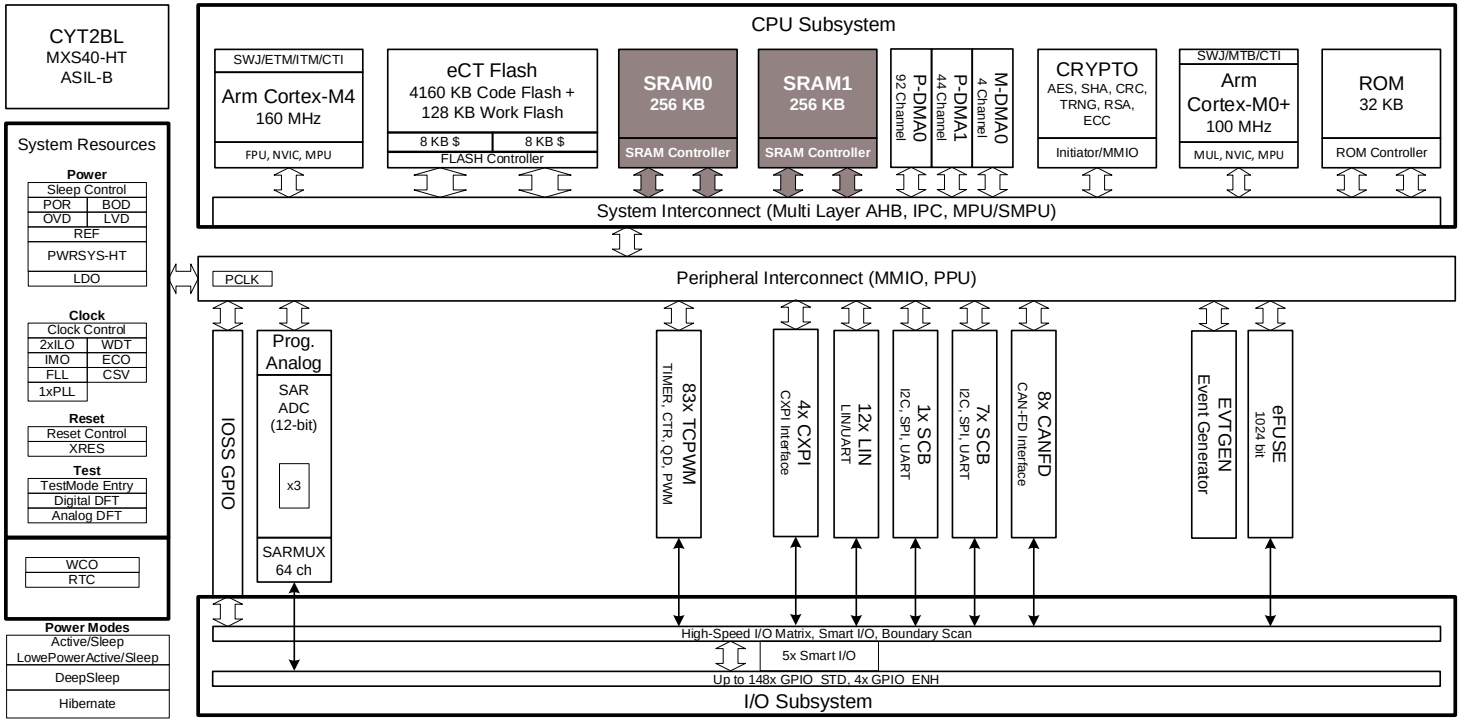
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160KB

Introduction to Traveo II Body Controller Entry

› SRAM interface is in the CPU subsystem



Hint Bar

Review TRM chapter 10 for additional details

Training section reference: SRAM Interface for Traveo II Body High

SRAM Interface Overview

- The SRAM controller in the SRAM memory interface has the following features:
  - Two AHB-Lite bus interfaces in two domains
    - Fast clock domain
    - Slow clock domain
  - Programmable wait states from 0 to 3
    - Wait states for the slow clock domain
      - In 0 wait cycle, up to 100 MHz of CLK_HF[1]
      - In 1 wait cycle, from 100 MHz to 160 MHz of CLK_HF
    - Wait states for the fast clock domain
      - In 0 wait cycle, up to 160 MHz of CLK_HF
  - 32-bit wide interface to SRAM memory
  - Error-correcting code (ECC)
  - Optional retention of SRAM contents in DeepSleep mode

Hint Bar

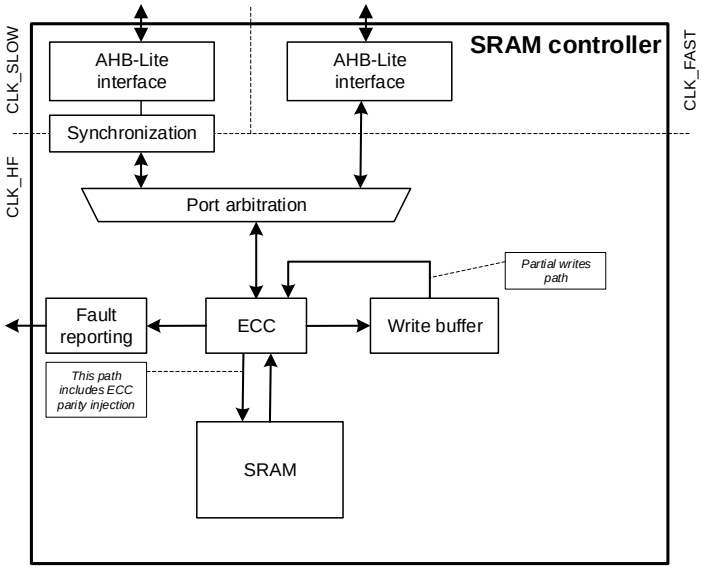
Review TRM chapter 10 for additional details

Review the Clock System Training section for additional details about high-frequency clocks

[1] High-frequency clock

SRAM Controller Block Diagram

- The SRAM controller consists of:
  - AHB-Lite interface
  - Synchronization
  - Port arbitration
  - Error-correcting code (ECC)
  - SRAM memory
  - Write buffer
  - Fault reporting

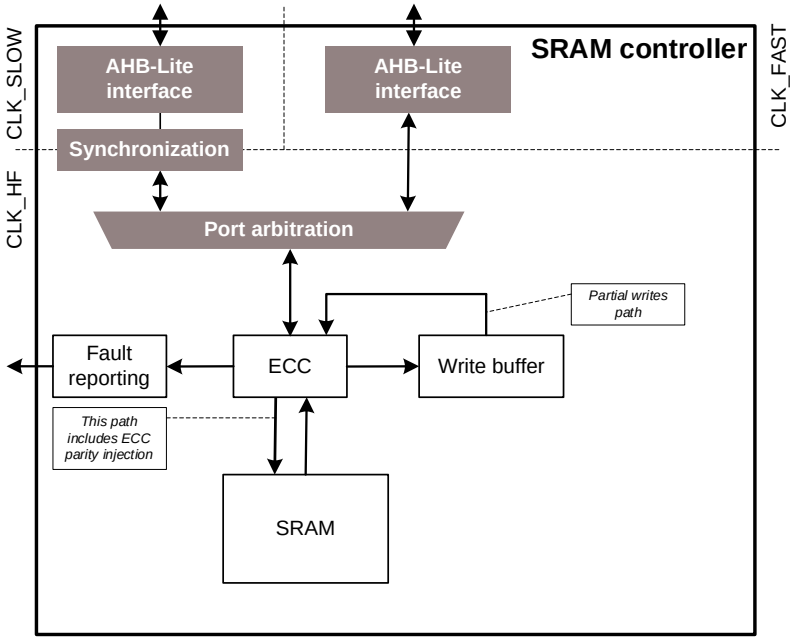


Hint Bar

Review TRM section 10.2 for additional details

AHB-Lite Interface

- The AHB-Lite interface includes:
  - AHB-Lite transfers
  - Arbitration priority



Hint Bar

Review TRM section 10.2 for additional details

AHB-Lite Transfers

- There are three types of AHB-Lite transfers
  - AHB-Lite read transfers
    - Translated into an SRAM read access
    - Uses ECC syndrome logic
  - 32-bit AHB-Lite write transfers
    - Translated into an SRAM write access
    - Uses ECC parity logic
  - Partial (8-bit and 16-bit) AHB-Lite write transfers
    - Translated into an SRAM read access and an SRAM write access
    - Only type that uses the write buffer

Hint Bar

Review TRM section 10.2 for additional details

Review the Error Correcting Code (ECC) section for additional details about ECC

Review the Write Buffer section for additional details about the Write Buffer

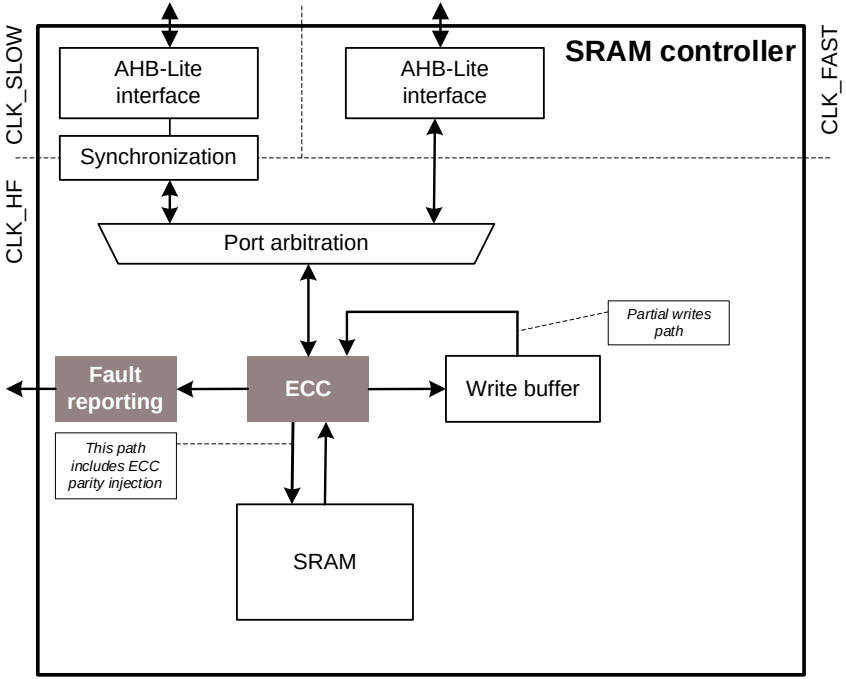
Arbitration Priority

- The arbiter component performs priority-based arbitration on the two AHB-Lite interfaces from the two interface ports
- The arbitration priority is set according to PROT_SMPU_MS0_CTL.PRIO register of SMPU (0 is highest, 3 is lowest)
- If Masters have the same priority, round-robin arbitration is performed according to the bus master identifier (starting from 15 to a lower identifier number)

Master Identifier	Bus Master
0	Arm® Cortex®-M0+
1	Cryptography component
2	P-DMA0
3	P-DMA1
4	M-DMA
14	Arm Cortex-M4
15	Test controller

Error-Correcting Code (ECC)

- ECC includes:
  - SECDED[1]
  - Fault reporting
  - Error injection



Hint Bar

Review TRM section 10.3 for additional details

[1] Single-error correction/double-error detection

ECC

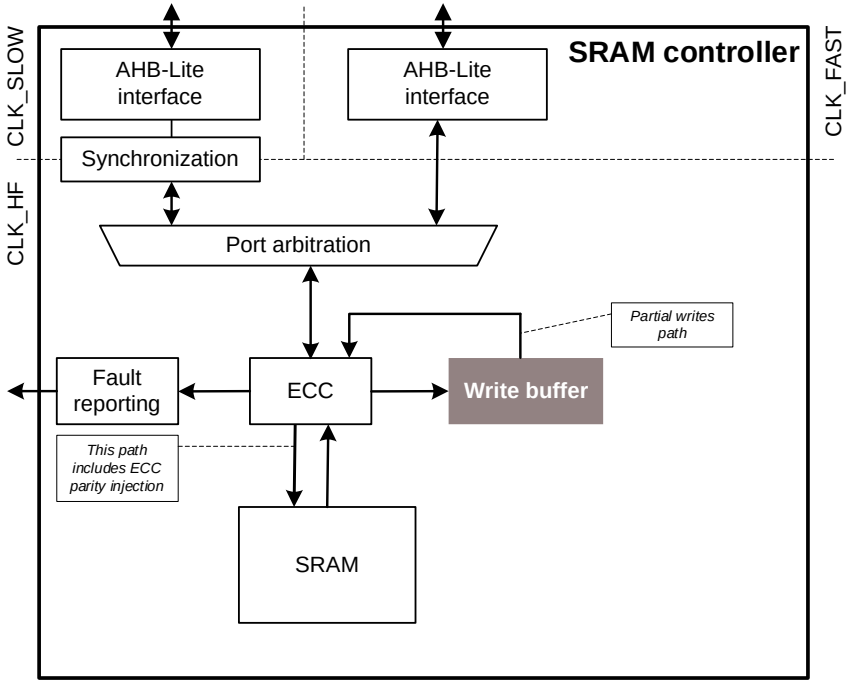
- SECDED
  - Corrects single-bit errors and detects double-bit errors
  - Reports error to the fault reporting structure
  - Includes 7-bit ECC per 32 bits of data and 25 bits of address
- Fault Reporting
  - Correctable and non-correctable ECC errors are reported to the fault structure in the same way
  - Use Case
    - SEC report: Log single-bit error count via the trigger that connects to TCPWM
    - DED report: Use for failsafe operations such as stop system control
- Error injection
  - Providing an error injection address and injection parity can generate an ECC error
  - Use Case
    - Use as initial diagnosis of ECC before running the application

Hint Bar

Review TRM section 10.3 for additional details

Write Buffer

- Write buffer request



Hint Bar

Review TRM section 10.2.4 for additional details

Write Buffer

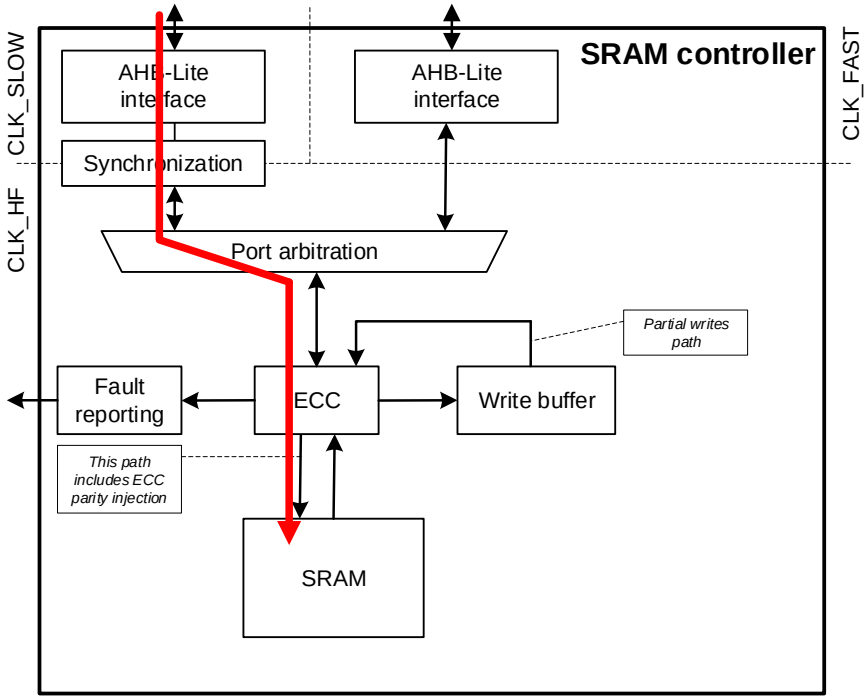
- The SRAM controller write buffer is used only when ECC is enabled
- 32-bit AHB-Lite write bus transfers require only a single SRAM write access
- Sequence of data merging involving the write buffer:
  - Requested read data is merged with partial write data to provide a complete 32-bit data word
  - Address and merged write data are written to the write buffer
  - A future write buffer request results in an SRAM write access with the merged write data
- For 8-bit and 16-bit AHB-Lite write bus transfers, an additional SRAM read access precedes the SRAM write access to retrieve the "missing" data bytes
- Since the write buffer is not retained in DeepSleep mode, empty the buffer before entering the mode
- The write buffer state is reflected as WB_EMPTY

Hint Bar

Review TRM section 10.2.4 for additional details

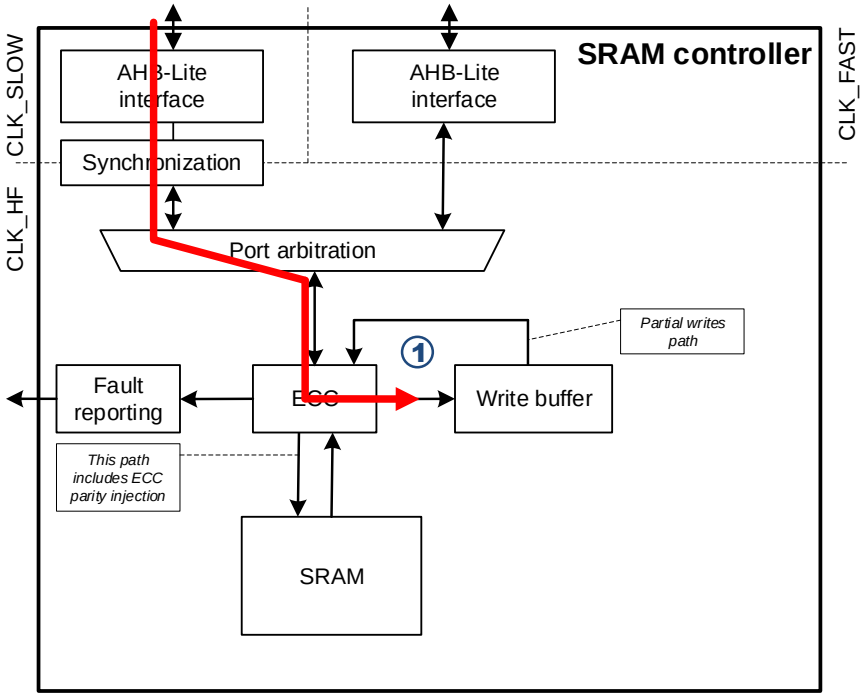
32-bit Write Buffer

› Only a single SRAM write access is required



8/16-bit Write Buffers, Partial Write with ECC (1/3)

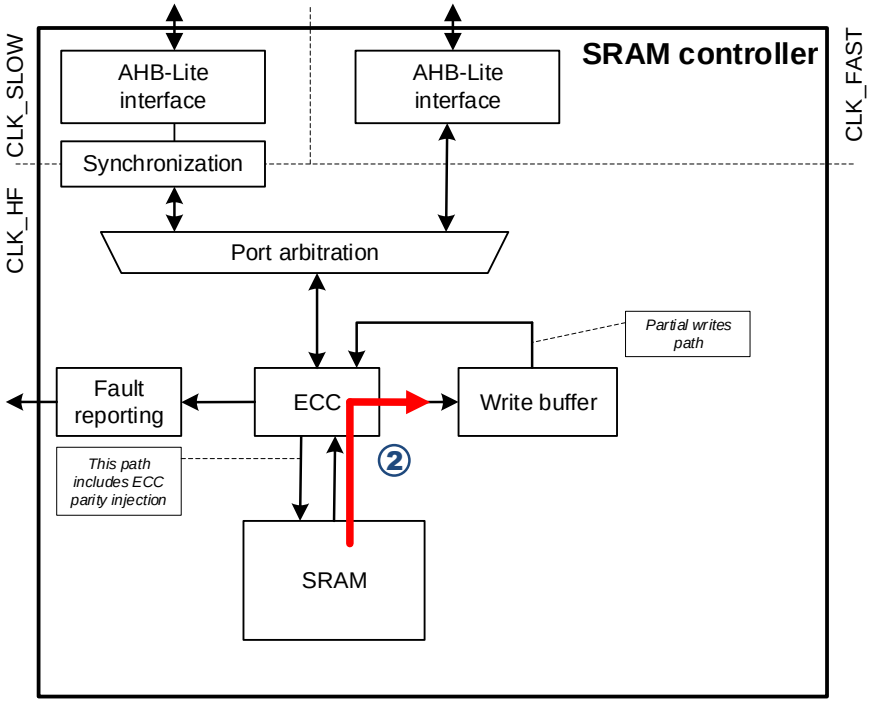
① Data from the AHB-Lite interface is stored in the write buffer



8/16-bit Write Buffers, Partial Write with ECC (2/3)

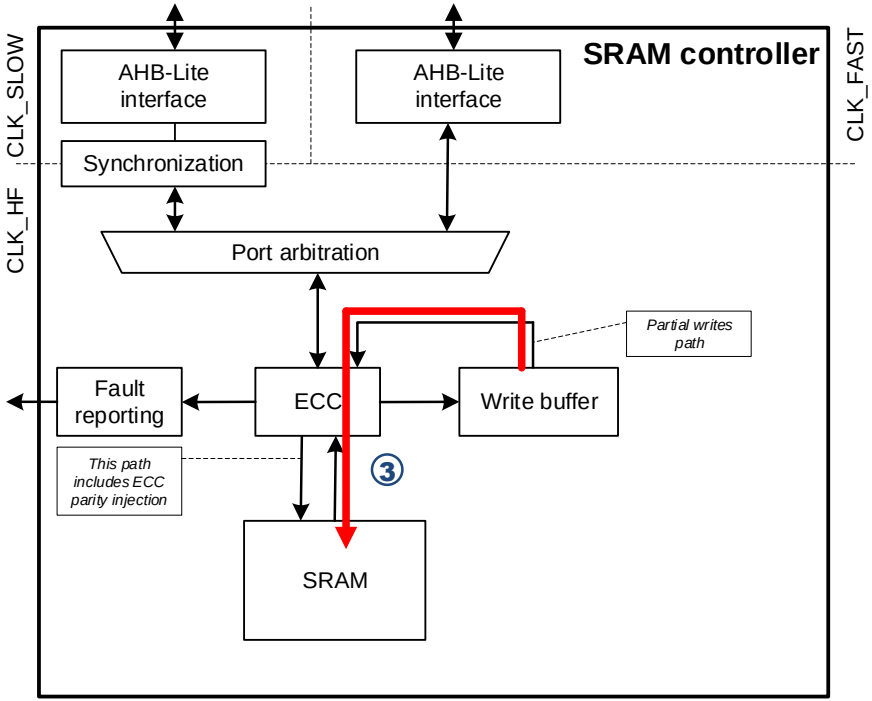
① Data from AHB-Lite interface is stored to the write buffer

② Missing data are read from SRAM and stored in the write buffer to complete the 32-bit word



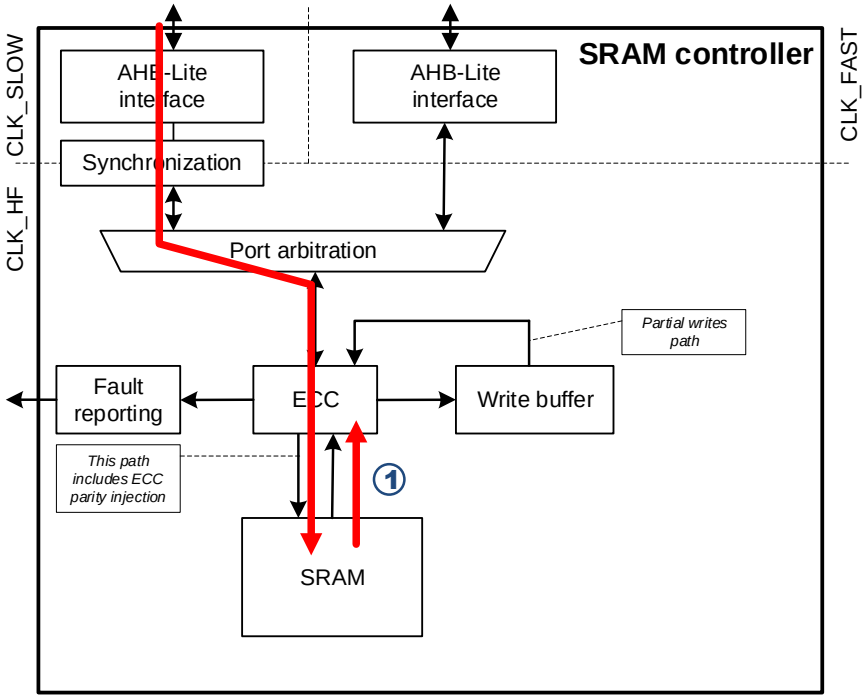
8/16-bit Write Buffers, Partial Write with ECC (3/3)

1. Data from AHB-Lite interface is stored to the write buffer
2. Missing data are read from SRAM and stored to the write buffer to complete the 32-bit word
3. Complete 32-bit word with ECC is written to the SRAM



Read With ECC with 1-bit Correctable Error (1/3)

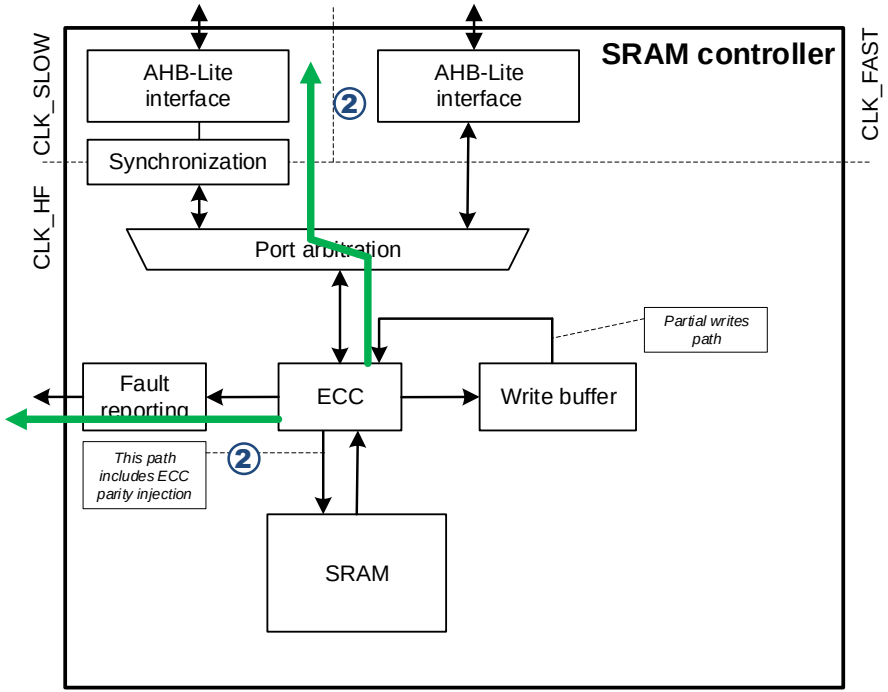
① 1-bit error is detected in AHB-Lite interface bus read data



Read With ECC with 1-bit Correctable Error (2/3)

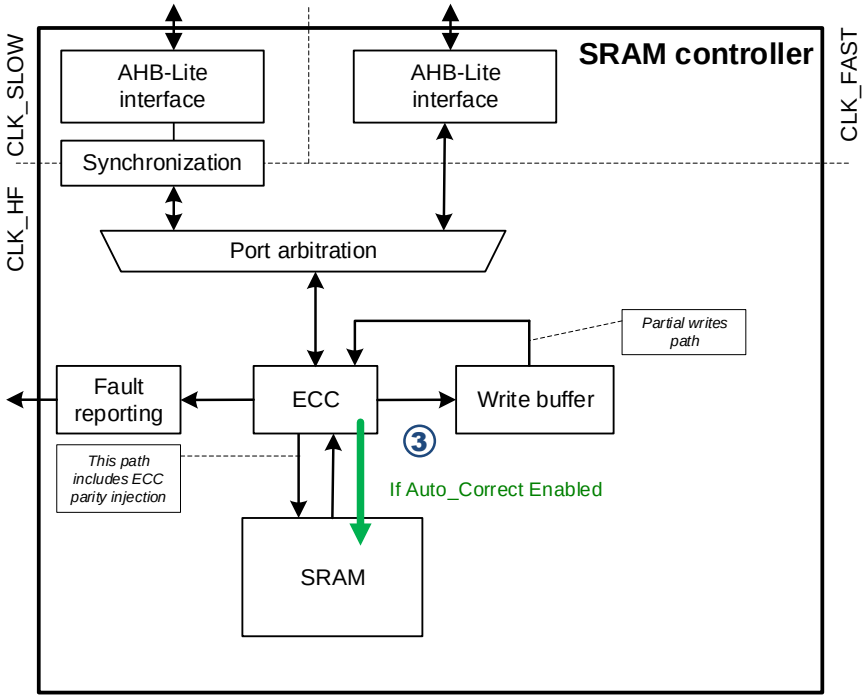
① 1-bit error is detected in AHB-Lite interface bus read data

② The error is notified to the fault reporting
The corrected data is sent to the AHB-Lite master requester



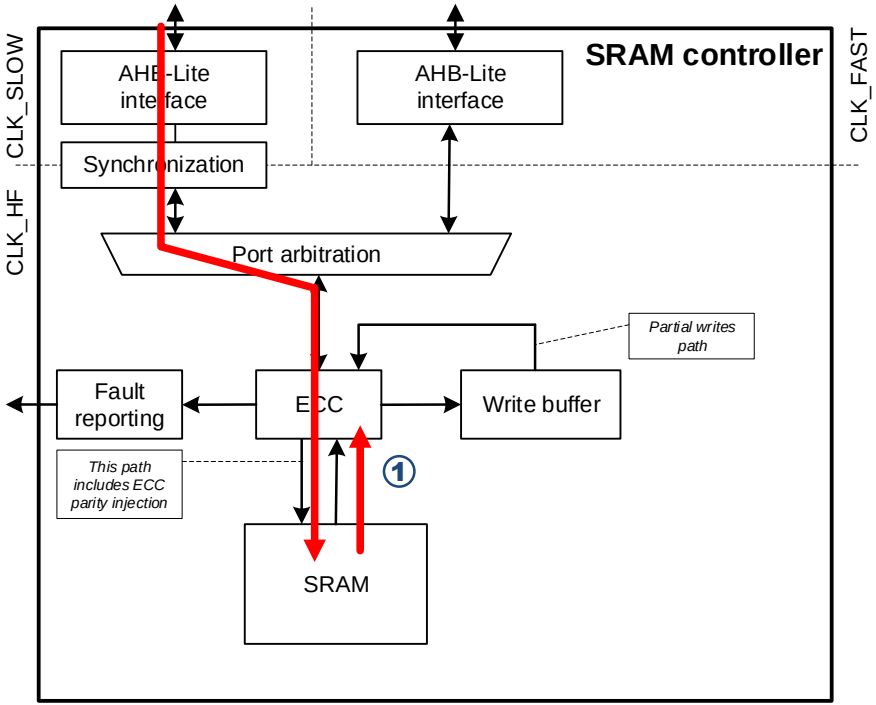
Read With ECC with 1-bit Correctable Error (3/3)

1. 1-bit error is detected in AHB-Lite interface bus read data
2. The error is notified to the fault reporting The corrected data is sent to the AHB-Lite master requester
3. If ECC_AUTO_CORRECT is enabled, the corrected data is written to the SRAM



Read With ECC with Non-Correctable Error (1/2)

① Non-correctable error is detected in AHB-Lite interface bus read data

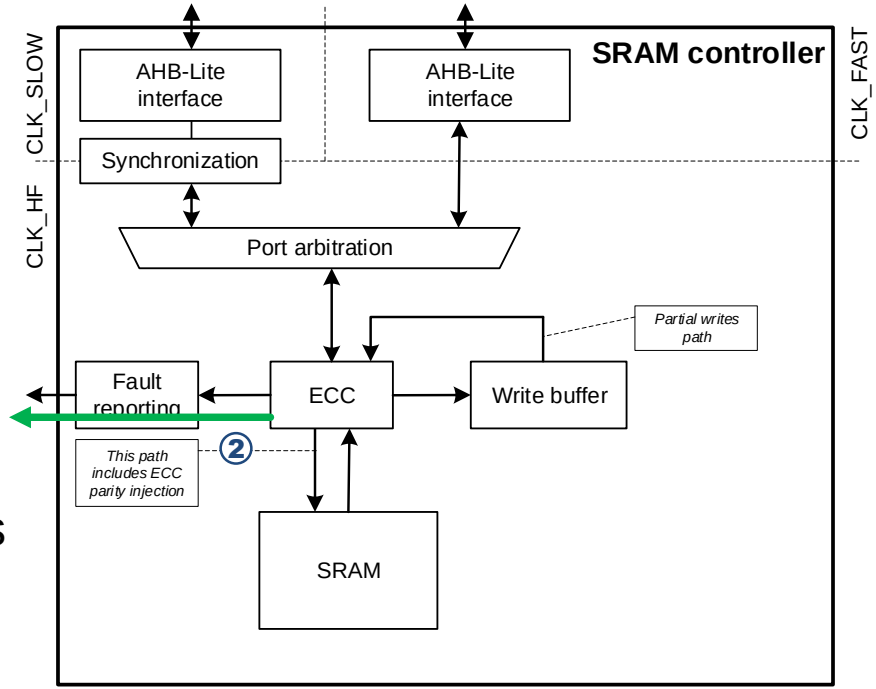


Read With ECC with Non-Correctable Error (2/2)

① Non- correctable error is detected in AHB-Lite interface bus read data

② The error is notified to the fault report

- Fault reporting captures the non-correctable error
  - Single-bit error detected in the word address
  - Double-bit error detected in the data access
- No bus error is detected while a fault is generated



SRAM Retention in DeepSleep

- In DeepSleep mode, SRAM0 can be fully retained or retained in increments of 32-KB sectors
- Advantage
  - By setting the size of backup RAM according to the system, it is possible to optimize the current consumption during DeepSleep mode

Hint Bar

SRAM unit other than SRAM0 can be fully retained

Review TRM section 10.1 for additional details on SRAM region that is not guaranteed to be retained across resets

Appendix

Comparison between CYT2BL, CYT4BF, and CYT4DN

Features		CYT2BL	CYT4BF	CYT4DN
SRAM	Memory size option	512KB	1024KB	640KB
	Interface width to SRAM memory	32-bit	64-bit	
	Bus interface	AHB-Lite	AHB-Lite, AXI	
	Wait states	Slow clock domain: 0 wait cycle for CLK_HF <= 100 MHz 1 wait cycle for 100 MHz < CLK_HF <= 160 MHz Fast clock domain: 0 wait cycle for CLK_HF <= 160 MHz	Slow clock domain: 0 wait cycle for CLK_MEM <= 100 MHz 1 wait cycle for 100 MHz < CLK_MEM <= 200 MHz Fast clock domain: 0 wait cycle for CLK_MEM <= 200 MHz	
	Bus master priority of arbiter	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 14: Cortex-M4 CPU 15: Test Controller	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 5: SDHC 9: Ethernet 0 10: Ethernet 1 13: Cortex-M7_1 CPU 14: Cortex-M7_0 CPU 15: Test Controller	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 9: Ethernet 0 12: Video Subsystem 13: Cortex-M7_1 CPU 14: Cortex-M7_0 CPU 15: Test Controller
	ECC (SED/DED)	Same		
	RAM retention in DeepSleep	Same		

Comparison between CYT2BL, CYT4BF, and CYT4DN

Features		CYT2BL	CYT4BF	CYT4DN
TCM	Memory size	N/A	16KB ITCM, 16KB DTCM	64KB ITCM, 64KB DTCM
	Interface width		ITCM: 64-bit D0TCM: 32-bit D1TCM: 32-bit	
	Bus interface		TCM interface	
	Wait states		Fast clock domain: 0 wait cycle for CLK_FAST <= 350 MHz	
	Priority		Cortex-M7 CPU only	
	ECC (SED/DED)		Supported	

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6140653	04/25/2018	Initial release
*A	6333945	10/05/2018	Added page 2, 4, Appendix section and the note descriptions of all pages. Updated page 3, 6, 7, 10, 12, 14, 15, 16, 17, 18, 19, 20, 21, 22.
*B	6633591	07/22/2019	Updated page 2, 24.
*C	7076348	01/27/2021	Updated page 1, 2, 3, 8, 22, and 24.