

Customer training workshop

TRAVEO™ T2G Body Entry CPU Subsystem
(CPUSS)

Q4 2021



Target products

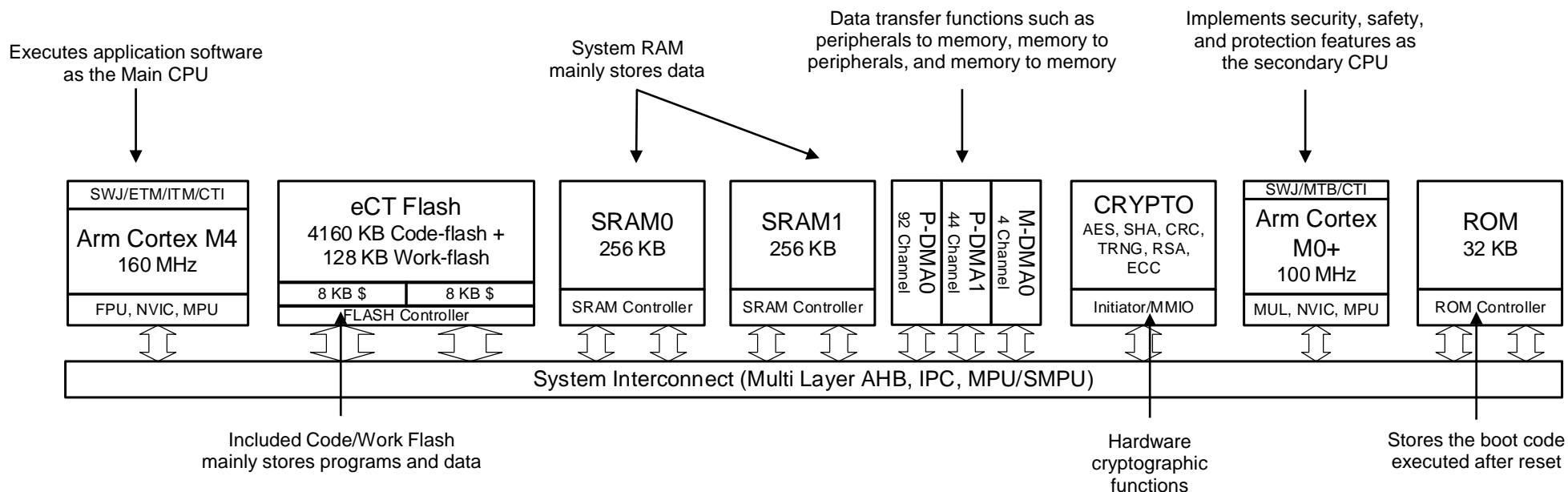
- › Target product list for this training material:

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B6	Up to 576 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2BL	Up to 4160 KB

CPU subsystem overview

- > The CPU subsystem (CPUSS) is based on dual 32-bit Arm[®] Cortex[®] CPUs

CPU subsystem components



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Review TRM section 4.1 for additional details specific to the CPUSS

Cortex[®]-M4 features summary

- > Main CPU
 - Execution of application software
 - Up to 160-MHz operation (CYT2BL)¹
- > System Tick (SysTick) timer
- > Floating-point unit (FPU)
 - Single precision
 - Compliant with the ANSI/IEEE Std 754-2008 IEEE Standard for Binary Floating-Point Arithmetic
- > Memory protection unit (MPU)
 - Eight protection regions
 - Privileged/unprivileged, read/write attributes
- > Nested vector interrupt controller (NVIC)
 - Eight external system interrupts, eight internal software interrupts, eight interrupt levels, and one non-maskable interrupt
 - Wakeup interrupt controller (WIC) support
 - Vector table relocation (VTOR)
- > Debug components
 - Supports SWD and JTAG interface (SWJ)
 - Tracing components (ETM, ITM, ETB)
 - Cross-triggering components (CTI)

Hint Bar

Arm[®] provides additional reference material on their webpage at: infocenter.arm.com

Training section references:

- Interrupts
- Program and Debug Interface
- Protection Units

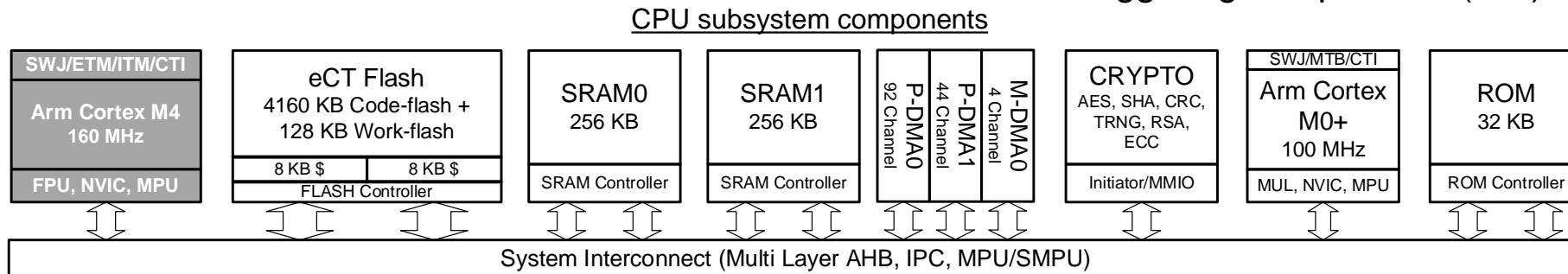
Combined SWD/JTAG interface (SWJ)

Embedded trace macrocell (ETM)

Instrumentation trace macrocell (ITM)

Cross-triggering interface (CTI)

Embedded trace buffer (ETB)



¹ See the device datasheet for operation frequency of target product.

Cortex[®]-M0+ features summary

- > Secondary CPU
 - Execution of boot process
 - Secure master in secure system to establish a root of trust
 - Up to 100-MHz operation (CYT2BL) ^{1, 2}
- > SysTick timer
- > Memory protection unit (MPU)
 - Eight protection regions
 - Privileged/unprivileged access attributes
- > Debug components
 - Supports SWD and JTAG interface (SWJ)
 - Tracing components (MTB)
 - Cross-triggering components (CTI)
- > Nested vector interrupt controller (NVIC)
 - Eight external system interrupts, eight internal software interrupts, four interrupt levels, and one non-maskable interrupt
 - Wakeup interrupt controller (WIC) support
 - Vector table relocation (VTOR)

Hint Bar

Arm[®] provides additional reference material on their webpage at: infocenter.arm.com

Training section references:

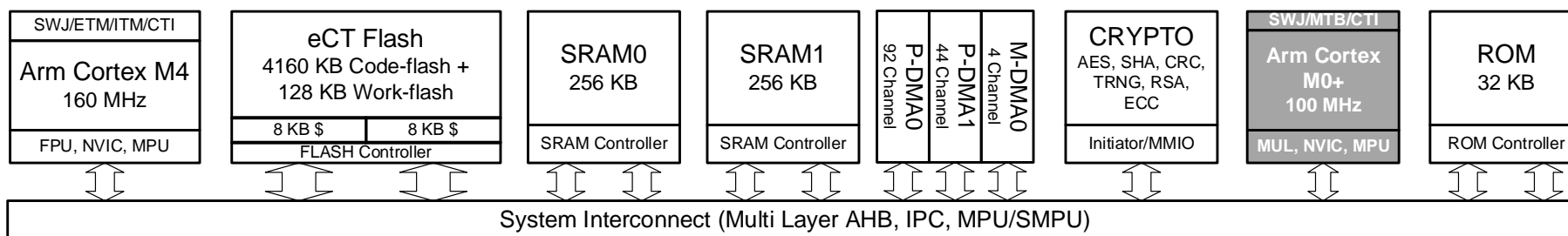
- Interrupts
- Program and Debug Interface
- Protection Units

Combined SWD/JTAG interface (SWJ)

Micro trace buffer (MTB)

Cross-triggering interface (CTI)

CPU subsystem components



¹ For CM4 to operate at 160 MHz, CM0+ is required to operate at a frequency of 80 MHz

² See the device datasheet for operation frequency of target product

CPUSS dedicated master identifier

- › Each bus master has a dedicated master identifier. This master identifier is used for:
 - Bus arbitration
 - IPC lock acquire functionality
 - Identification of access violated bus master detected by MPU, SMPU, and PPU

Master identifier ¹	Bus master (CYT2BL)
0	Cortex [®] -M0+
1	Crypto
2	P-DMA 0
3	P-DMA 1
4	M-DMA
14	Cortex-M4
15	Test Controller

¹See the device datasheet for master identifier number and regarding peripherals of target product

Hint Bar
Inter processor communication (IPC)
Memory protection unit (MPU)
Shared memory protection unit (SMPU)
Peripheral protection unit (PPU)

CPUSS bus infrastructure

- > AHB-Lite bus infrastructure
- > Two clock domains
 - Fast and slow clock domains
 - Each memory interface has both clock domains
 - Each domain has a dedicated bus infrastructure
- > Bus competition
 - CPUSS has multiple bus masters
 - Design a system that considers bus competition by simultaneous access

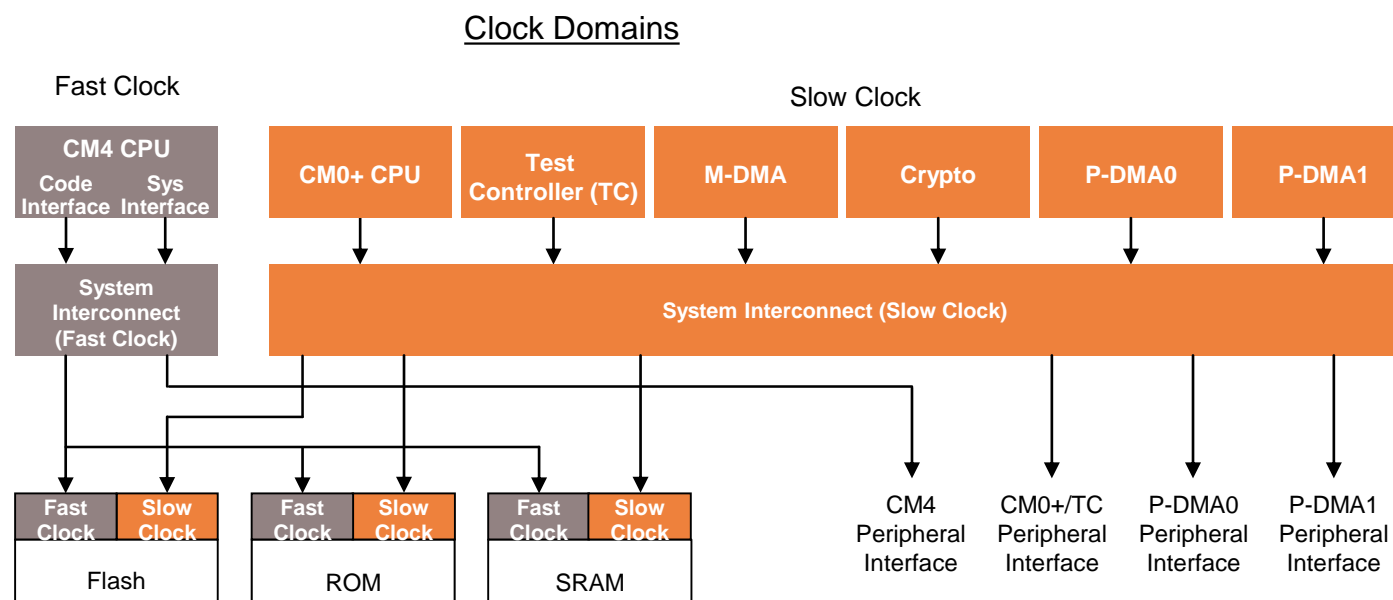
Hint Bar

Sys Interface in CM4 can only access peripherals

Code Interface in CM4 can only access memory controllers

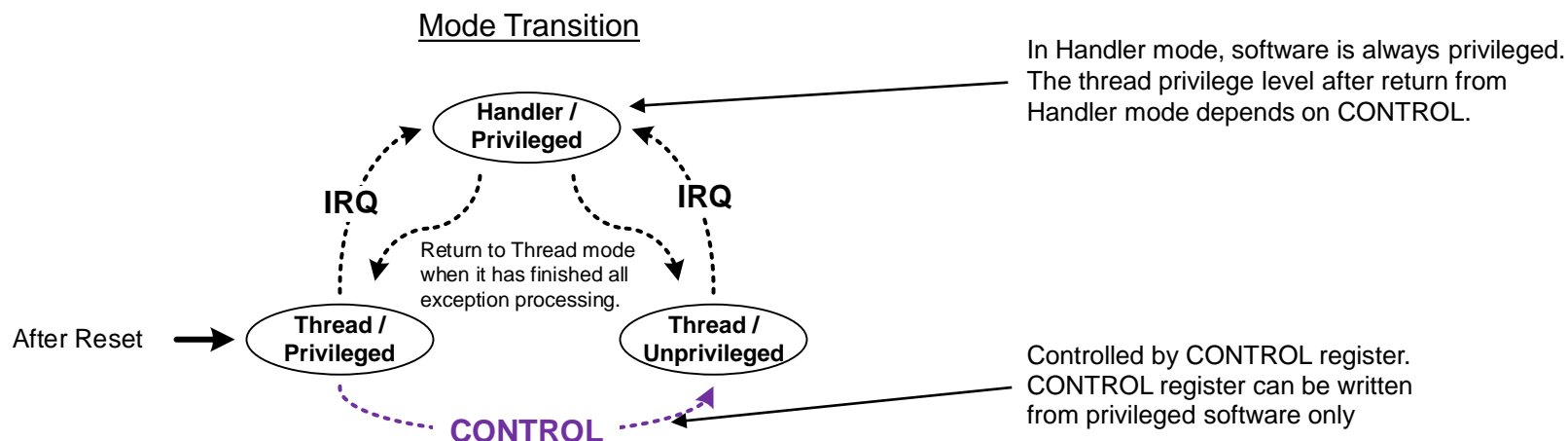
Training section references:

- **Clock system**



CPU mode transition

- › Both CPUs support two operating modes and two privilege levels
 - Operating mode
 - Thread mode executes application software and Handler mode handles exceptions
- › Privilege levels
 - Unprivileged: Software has limited access to MSR/MRS instructions (uses CPS instructions), system timer, NVIC, system control block, and memory/peripherals
 - Privileged: Software can use all instructions and has access to all resources
 - Transition from Thread/Privileged to Thread/Unprivileged by CONTROL register¹
 - Transition from Thread/Unprivileged to Thread/Privileged via SVC²



Hint Bar

Review TRM section 4.5 for additional details specific to CPU Modes

Arm provides additional reference material on their webpage at: infocenter.arm.com

Move to system coprocessor register from Arm register (MSR)

Move the contents of a program status register to a general-purpose register (MRS)

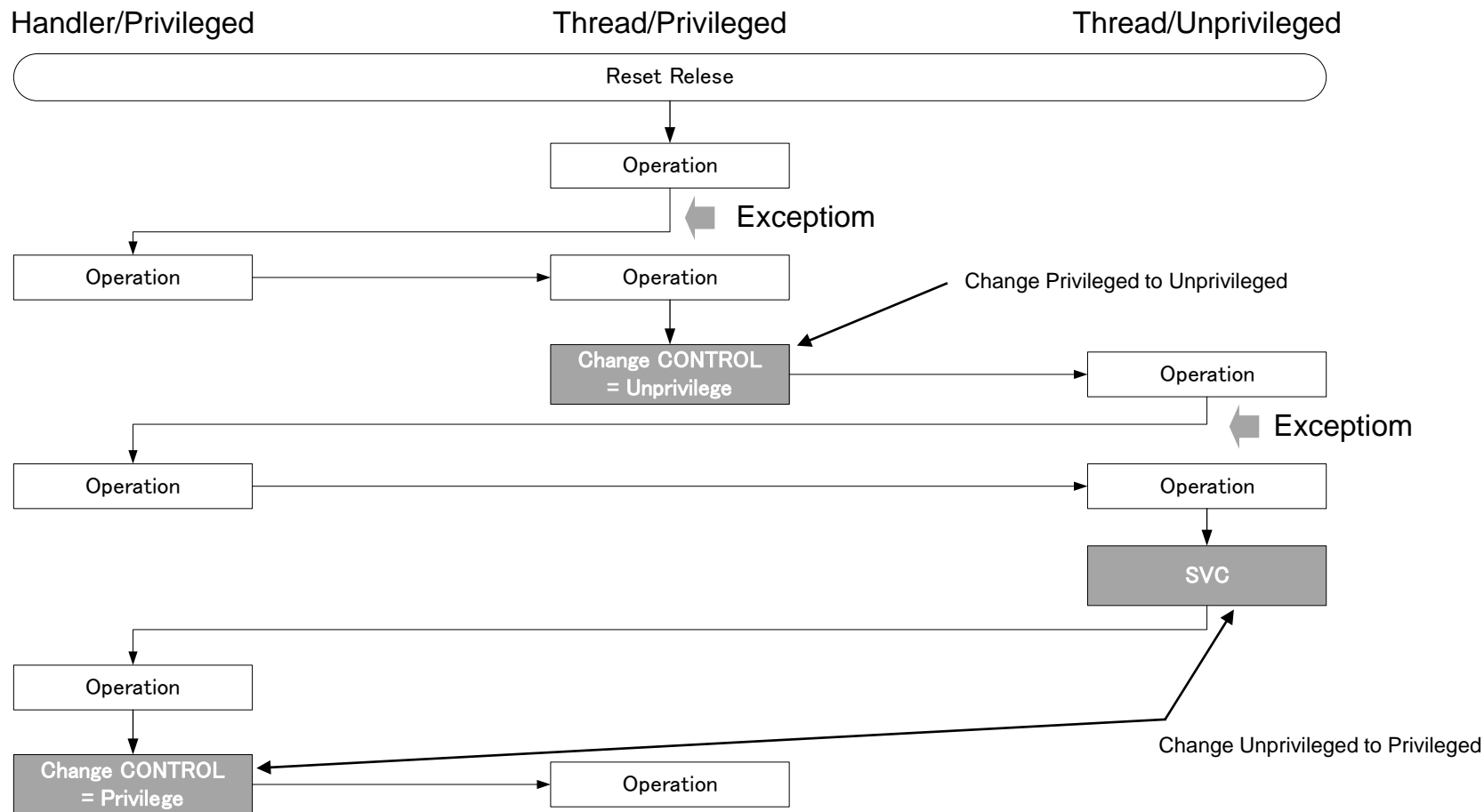
Change processor state (CPS)

¹ The CONTROL register is a CPU-specific register. It defines privileged/unprivileged, stack pointer, and FPU extension.

² Supervisor calls are used to request privileged operations

Operation modes transition

> Use case: Changing Privileged/Unprivileged mode



Hint Bar

Arm provides additional reference material on their webpage at: infocenter.arm.com

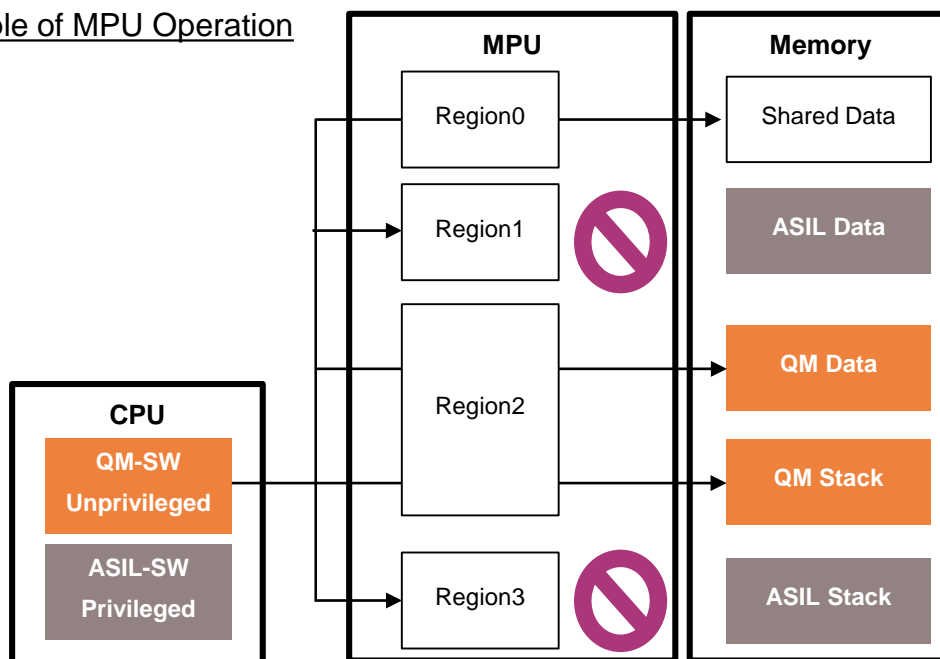
Memory protection

- > Both CPUs have a memory protection unit (MPU)¹ that:
 - Recognizes software separation
 - Includes address range, read/write, and privileged/unprivileged attributes
 - Features eight protection regions
- > Use case
 - Software partitioning of ASIL and QM in functional safety

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Arm provides additional reference material on their webpage at: infocenter.arm.com

Example of MPU Operation

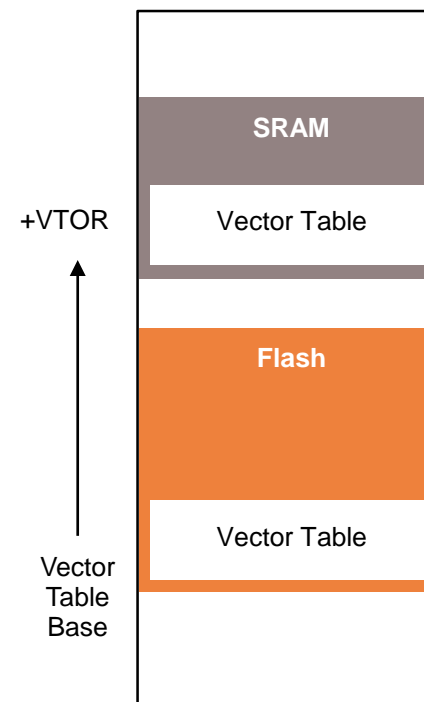


¹ MPU registers are written by Privileged software and are only one part of the protection concept. For details, see the Protection Units training section.

Vector table relocation

- > Vector table offset register (VTOR)¹
 - Defines the location of the vector table of each core. There is a VTOR for CM4 and another one for CM0.
 - Can be used to relocate the vector table from Flash to SRAM, allowing the interrupt handlers to change dynamically
 - VTOR is written from Privileged software only
 - Boot ROM uses the sets the VTOR of CM0+, and CM0+ sets the VTOR of CM4:
 - CM0_VECTOR_TABLE_BASE: By default, set to beginning of Flash
 - CM4_VECTOR_TABLE_BASE: Set by CM0+ before releasing CM4 from reset
 - After boot, each core copies the vector table to SRAM and updates VTOR with the address of the new location
- > Use cases
 - Execute the program with RAM only, for Flash programming or performance improvement
 - Use different vectors depending on the software level or system mode, such as normal and reprogramming

VTOR Operation



Hint Bar

Arm provides additional supporting material on their webpage at: infocenter.arm.com

See the Register TRM for additional details

¹ The VTOR register is a CPU-specific register.

System tick generation

- › Both CPUs support a SysTick timer to measure time duration, which provides:
 - A 24-bit down counter
 - A selectable internal CPU clock or external clock
 - Active and Sleep mode operation
 - SysTick interrupt generation
- › SysTick registers can be written from Privileged software only
- › Use cases
 - RTOS tick timer
 - Alarm timer to alert when an action is not completed within a particular duration
 - Software completion time measurement

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Arm provides additional supporting material on their webpage at: infocenter.arm.com

CPU subsystem memory feature summary

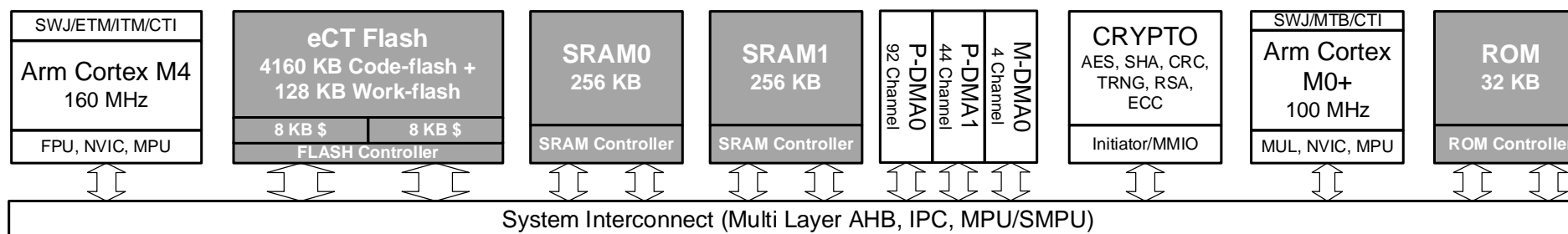
- › Flash
 - Code and work flash
 - Code flash: Up to 4MB (CYT2BL)¹
 - Work flash: Up to 128KB (CYT2BL)¹
- › Error-correction code (ECC) function (SECDED)
- › Instruction cache for both CPUs
- › APIs for flash programming
- › SRAM
 - Data storage and code execution
 - Up to 512KB (CYT2BL)¹
 - Dual CPU sharing
 - ECC function
- › ROM
 - Boot code for both cores
 - API² function implementation

Hint Bar

Training section references:

- Flash
- SRAM interface
- Boot

CPU subsystem components



¹ See the device datasheet for memory size of target product.

² No user access to read or modify SROM code

P-DMA/M-DMA feature summary

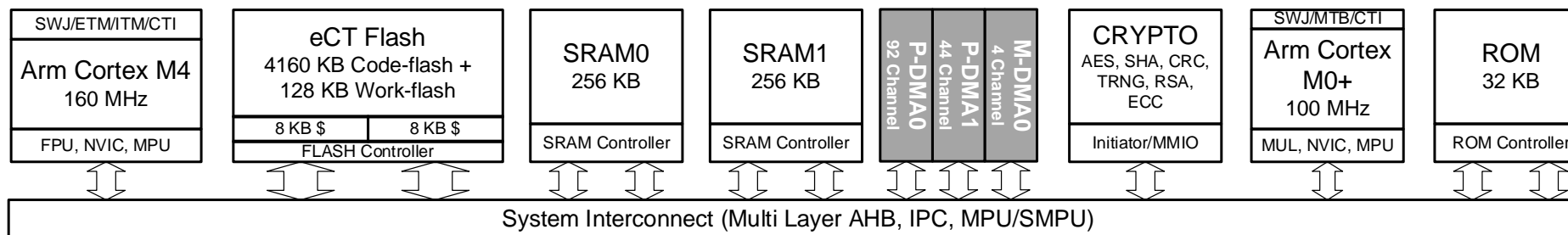
- > Peripheral DMA (P-DMA)
 - Single transfer engine shared for all channels
 - Focuses on low-latency transfer
 - Transfer modes:
 - Single, 1D, 2D, and CRC
- > Memory DMA (M-DMA)
 - Dedicated transfer engine for each channel
 - Focuses on high-memory bandwidth
 - Transfer modes:
 - Single, 1D, 2D, Memory Copy, and Scatter

Hint Bar

Training section references:

- Direct Memory Access

CPU Subsystem Components



Cryptographic (Crypto) feature summary

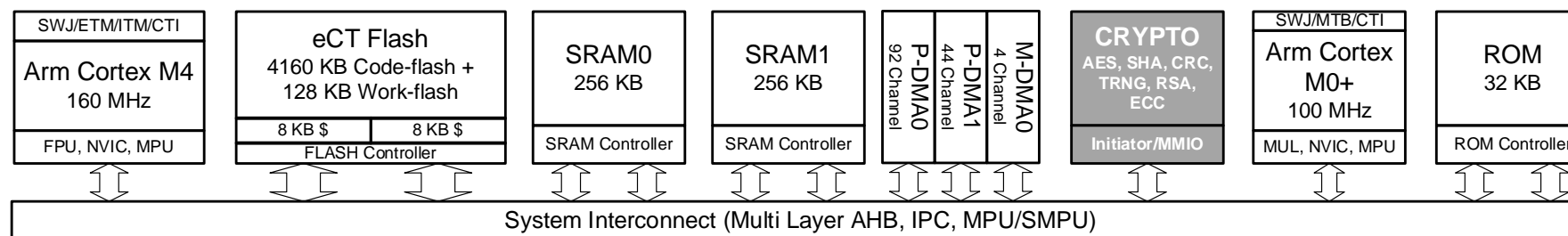
- > Hardware crypto functions¹
 - Symmetric key encryption and decryption
 - Hashing
 - Message authentication
 - Random number generation
 - Cyclic redundancy checking
 - Asymmetric key cryptography

Hint Bar

Training section references:

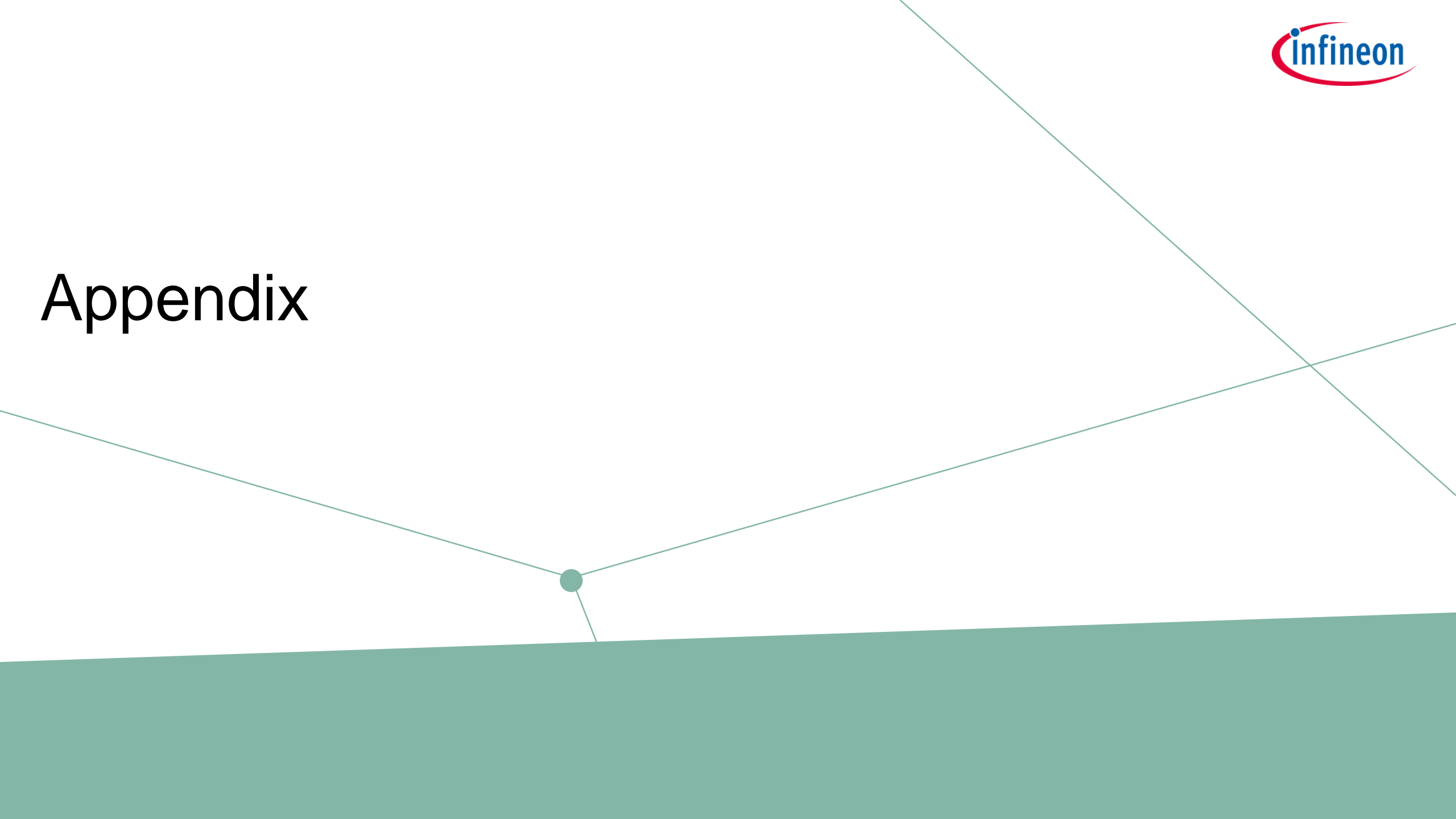
- Device Security

CPU subsystem components



¹ Access limited to the secure master (CM0+)

Appendix



Comparison between families

Features		Body Controller Entry (CYT2BL)	Body Controller High (CYT4BF)	Cluster (CYT4DN)
Main CPU	CPU	Cortex-M4 CPU	Two Cortex-M7 CPUs	
	Operating Frequency	Up to 160 MHz	Up to 350 MHz	Up to 320 MHz
	FPU	Single-precision	Single/double-precision	
	Cache	N/A	16KB instruction, 16KB data	
	MPU	Cortex-M4: 8 regions	Cortex-M7: 16 regions	
	Interrupt Structure	NVIC+WIC		
	System Tick Timer	Supported		
Secondary CPU	CPU	Cortex-M0+ CPU		
	Operating Frequency	Same (Up to 100 MHz)		
	MPU	Cortex-M0+: 8 regions		
	Interrupt Structure	NVIC+WIC		
	System Tick Timer	Supported		
Flash	Bus Interface	AHB-Lite	AXI, AHB-Lite	
	ECC (SEC/DED)	Supported		
	Bank Modes	Supported		
	Size (Code/Work)	4MB / 128KB	8MB / 256KB	6MB / 128KB
SRAM	Bus Interface	AHB-Lite	AXI, AHB-Lite	
	ECC (SEC/DED)	Support		
	TCM Size	N/A	16KB ITCM, 16KB DTCM	64KB ITCM, 64KB DTCM
	SRAM Size	512KB	1024KB	640KB
Boot		Supported		
Device Security with Crypto		Supported		
Direct Memory Access	P-DMA	Supported		
	M-DMA	Supported		



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Revision History

Revision	ECN	Submission Date	Description of Change
**	6084432	03/12/2018	Initial release
*A	6390381	11/21/2018	Added slide 2 Updated slides 2-4, 6, 12-14. Deleted inside cover Deleted slides 16,17,18
*B	7060645	01/06/2021	Updated slides 2-6, 13-15, 17.
*C	7450302	11/16/2021	Update slides 11