Customer training workshop

TRAVEO™ T2G Automotive Body Controller Entry/High and Cluster family overview

Q1, 2024

Target products

› Target product list for this training material:

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B6	Up to 576 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2BL	Up to 4160 KB
TRAVEO™ T2G Automotive Body Controller High	CYT3BB/4BB	Up to 4160 KB
TRAVEO™ T2G Automotive Body Controller High	CYT4BF	Up to 8384 KB
TRAVEO™ T2G Automotive Body Controller High	CYT6BJ	Up to 16768 KB
TRAVEO™ T2G Automotive Cluster Entry	CYT2CL	Up to 4160 KB
TRAVEO™ T2G Automotive Cluster 2D	CYT3DL	Up to 4160 KB
TRAVEO™ T2G Automotive Cluster 2D	CYT4DN	Up to 6336 KB

TRAVEO™ T2G Body Controller Entry

Overview

- Includes Arm® Cortex ® -M4F and Cortex®-M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (such as body control units)
- Features
  - 32-bit CPU subsystem:
    - 160-MHz[1] Cortex®-M4F CPU with single-cycle multiply, single precision floating-point unit (FPU), and memory protection unit (MPU)
    - 100-MHz[2] Cortex®-M0+ CPU with MPU
  - CYT2B6: Up to 576KB of Code Flash along with 64KB of Work Flash
  - CYT2B7: Up to 1088KB of Code Flash along with 96KB of Work Flash
  - CYT2B9: Up to 2112KB of Code Flash along with 128KB of Work Flash
  - CYT2BL: Up to 4160KB of Code Flash along with 128KB of Work Flash
    - Dual Bank Mode support for Firmware Over-the-Air (FOTA)
  - SRAM: CYT2B6: up to 64KB, CYT2B7: up to 128KB, CYT2B9: up to 256KB, CYT2BL: up to 512KB
  - Internal 8-MHz main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Low-power 2.7 to 5.5 V operation
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support

Hint Bar

Review datasheet and TRM chapter 1 for additional details

[1] CYT2B6 up to 80-MHz
[2] CYT2B6 up to 80-MHz

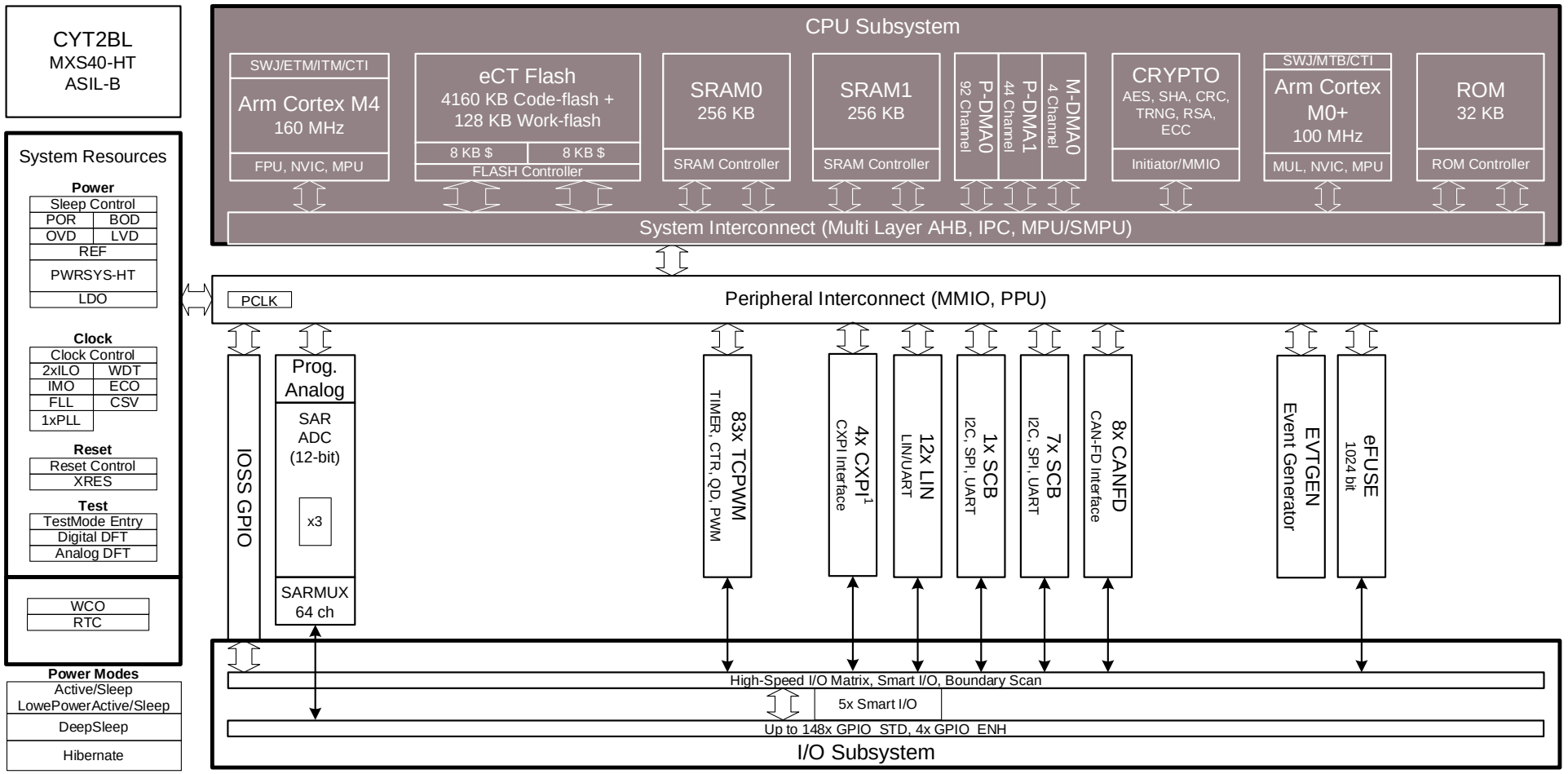
Overview

- Features (continued)
  - AEC-Q100 qualification and ASIL-B level functional safety
  - Debugging via SWD/JTAG controller and interface-compliant IEEE-1149.1-2001, and Flash programming on the SWD/JTAG interface
  - Packages:
    - 64-/80-/100-/144-/176-LQFP packages available for CYT2B7/B9/BL
    - 64-/80-/100-LQFP packages available for CYT2B6

Hint Bar

Review datasheet and TRM chapter 1 for additional details

CYT2BL architecture diagram: CPU subsystem

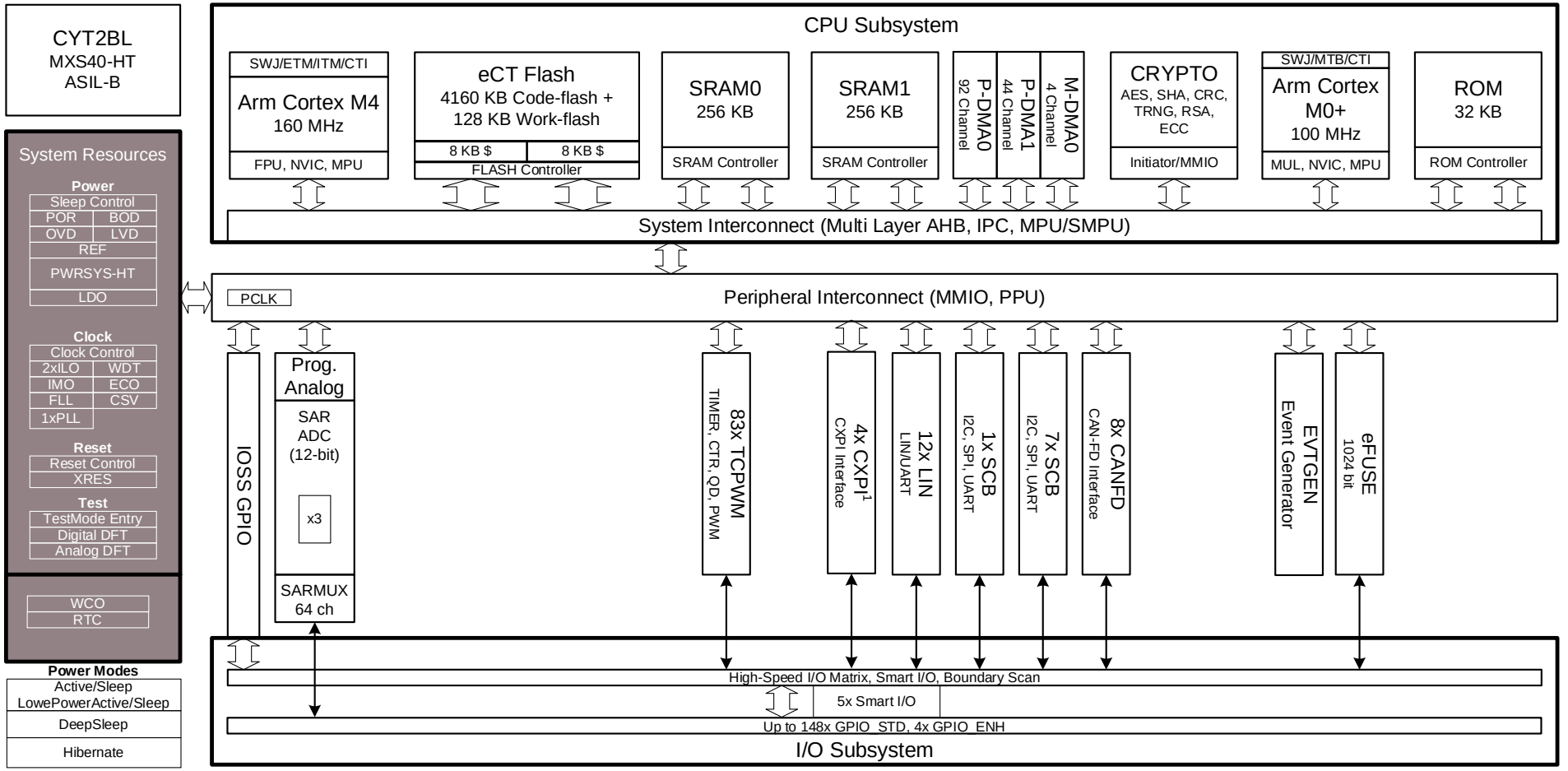


Hint Bar

Training section reference

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

CYT2BL architecture diagram: System resources



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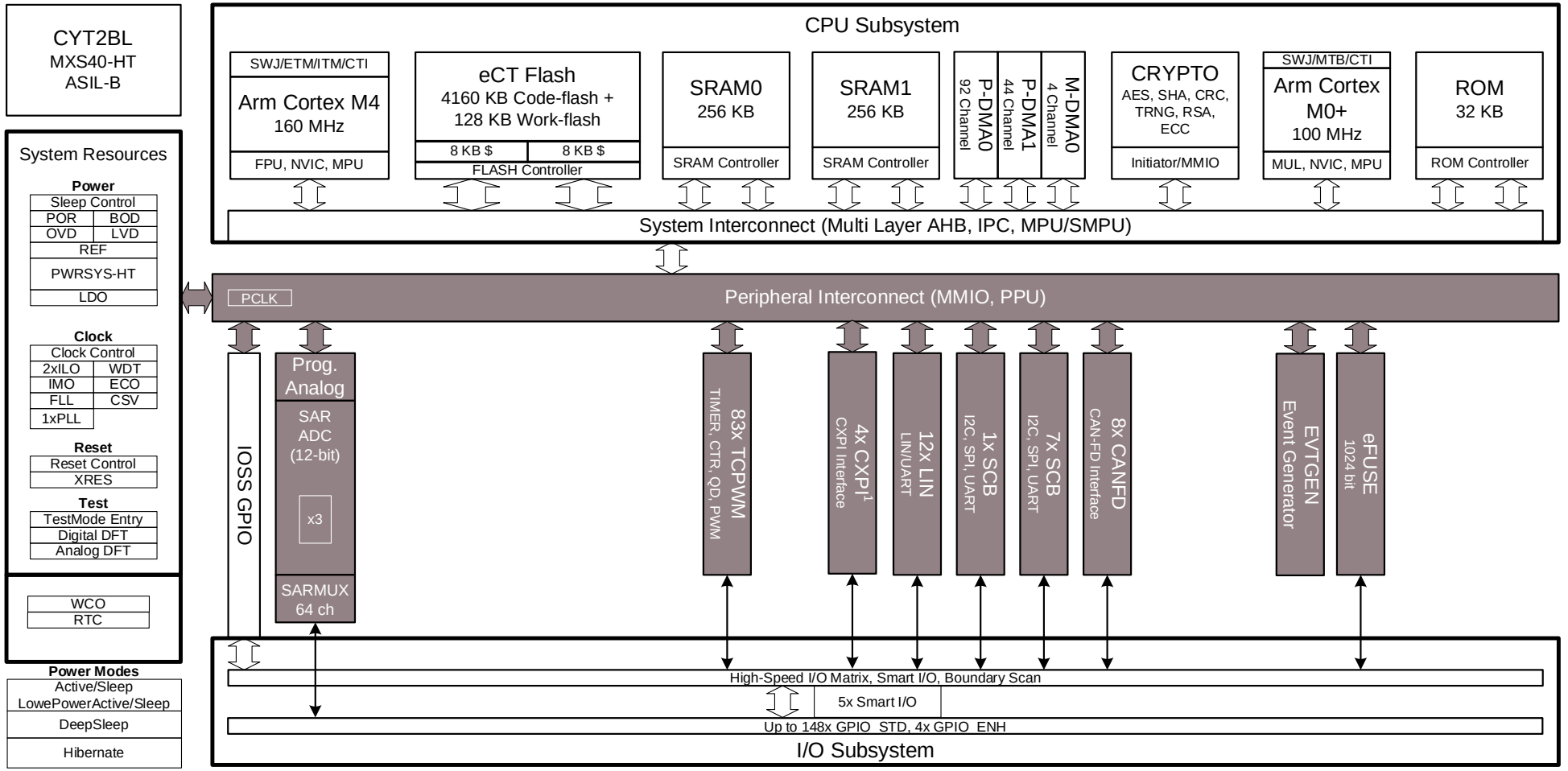
Training section reference

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

CYT2BL architecture diagram: Peripheral blocks

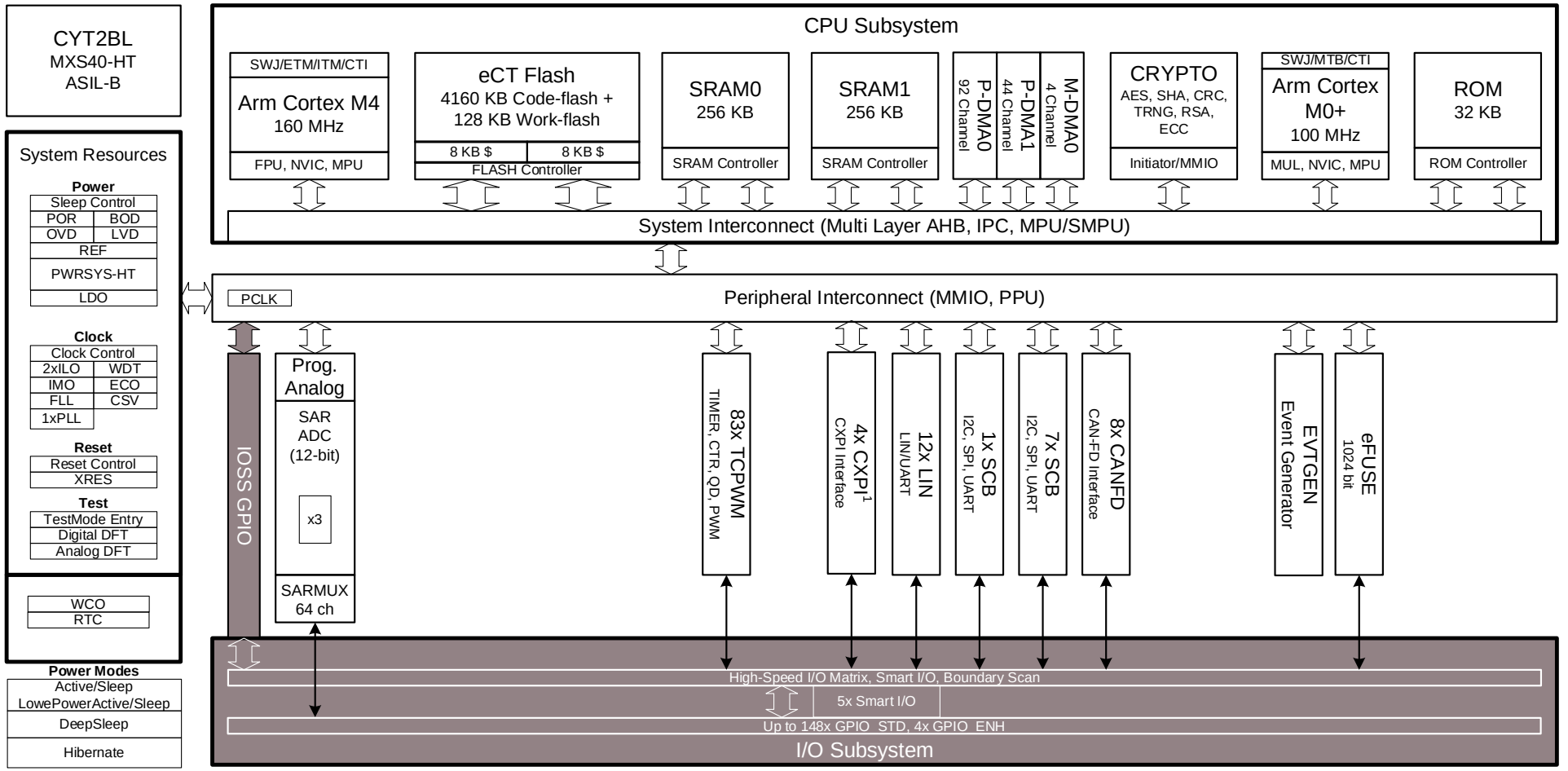


Hint Bar

Training section reference

- **SAR ADC**
- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **CXPI**

CYT2BL architecture diagram: I/O subsystem



Hint Bar

Training section reference
- I/O Subsystem

TRAVEO™ T2G Body Controller High

Overview

- Includes Arm® single/dual Cortex®-M7 and Cortex®-M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (gateway, high-end body-control units, etc.)
- Features
  - 32-bit CPU subsystem:
    - CYT3BB: One 250-MHz Cortex®-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
    - CYT4BB: Two 250-MHz Cortex®-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
    - CYT4BF: Two 350-MHz Cortex®-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
    - CYT6BJ: Four 320-MHz Cortex®-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
    - 100-MHz Cortex®-M0+ CPU with MPU (all devices)
  - CYT3BB/4BB: 4160KB of Code Flash along with 256KB of Work Flash:
  - CYT4BF: 8384KB of Code Flash along with 256KB of Work Flash:
  - CYT6BJ: 16768KB of Code Flash along with 512KB of Work Flash:
    - Dual Bank Mode support for Firmware Over-the-Air (FOTA)
  - SRAM: CYT3BB/4BB: 768KB, CYT4BF: 1024KB, CYT6BJ: 2048KB
  - Internal 8-MHz main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  - External (> 300 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD = 1.15 V

Hint Bar

Review datasheet and TRM chapter 1 for additional details

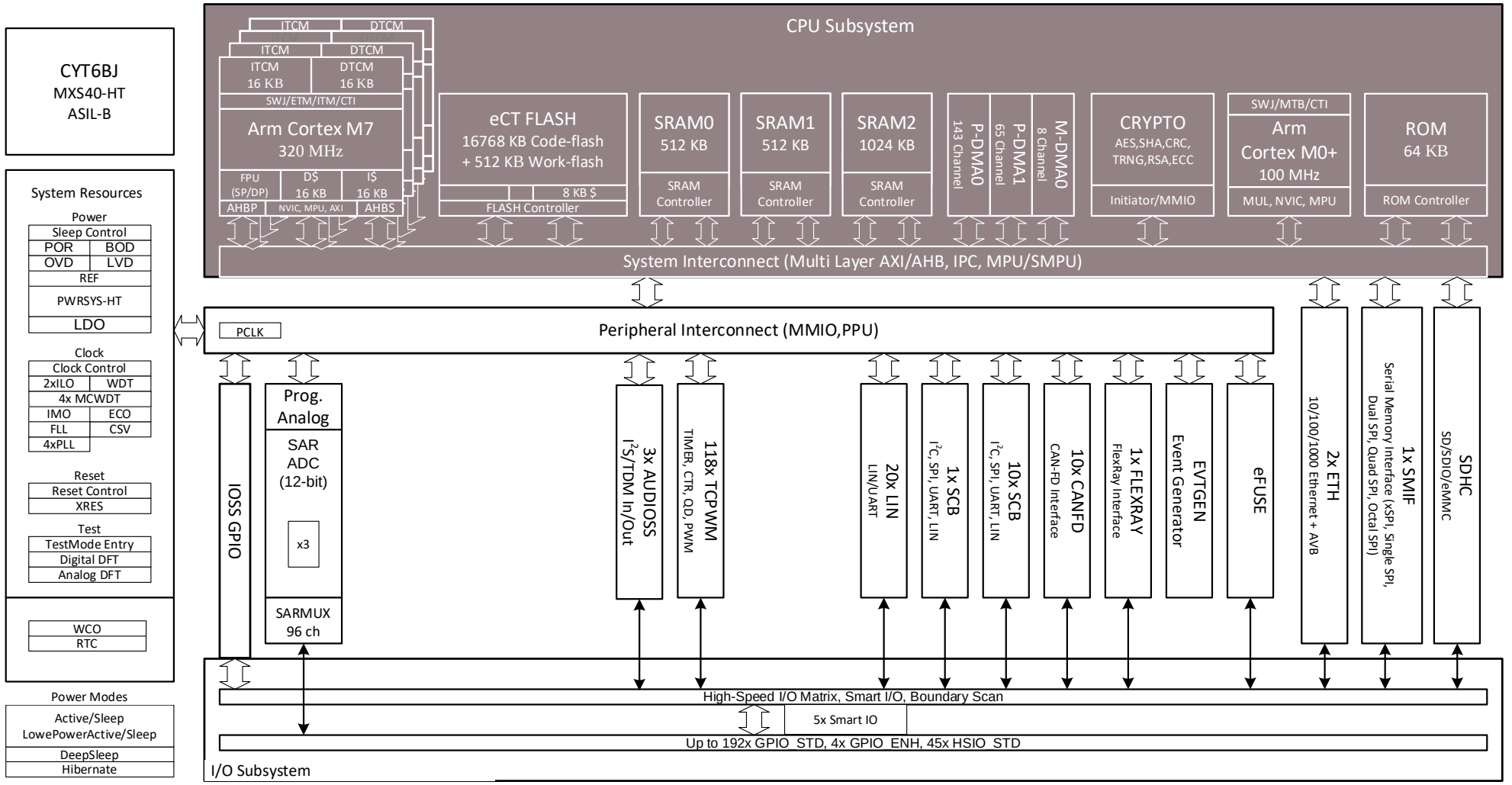
Overview

- Features (continued)
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support
  - AEC-Q100 qualification and ASIL-B level functional safety
  - Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface
  - Packages:
    - CYT3BB/4BB: 100-/144-/176-TEQFP, 272-FBGA packages available
    - CYT4BF/6BJ: 176-TEQFP, 272-FBGA, 320-BGA packages available

Hint Bar

Review datasheet and TRM chapter 1 for additional details

CYT6BJ architecture diagram: CPU subsystem

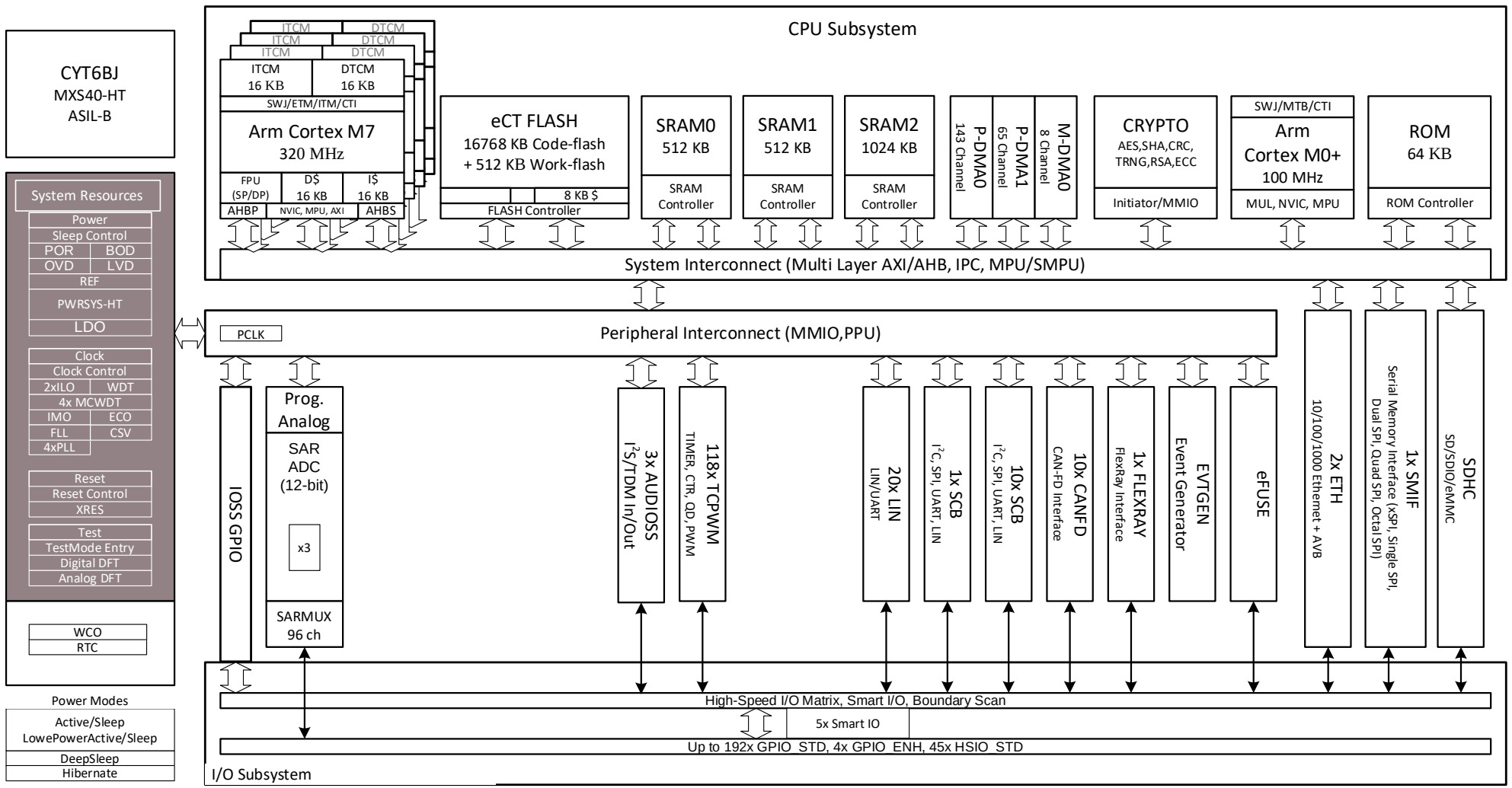


Hint Bar

Training section reference

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

CYT6BJ architecture diagram: System resources

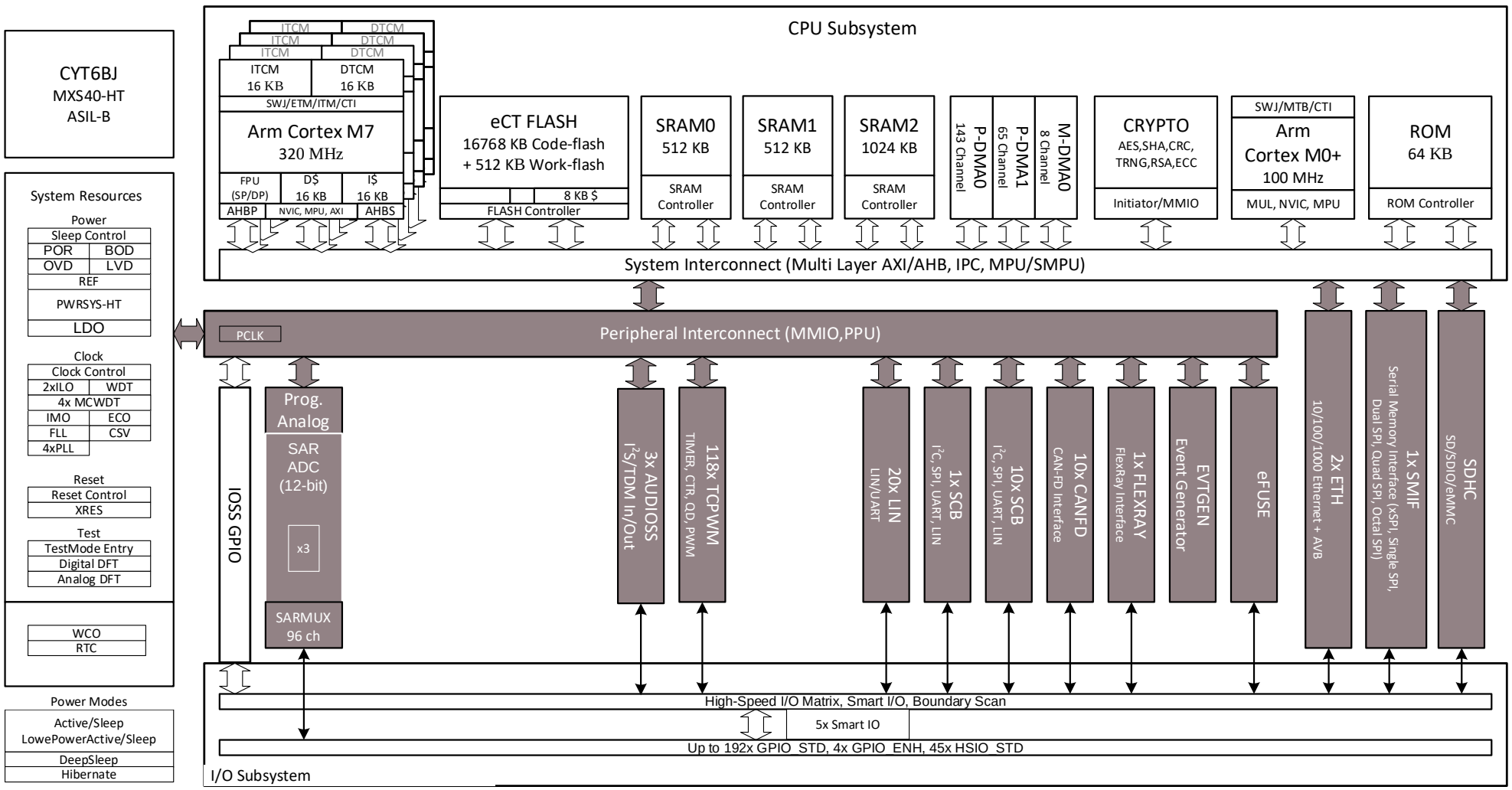


Hint Bar

Training section reference

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

CYT6BJ architecture diagram: Peripheral blocks

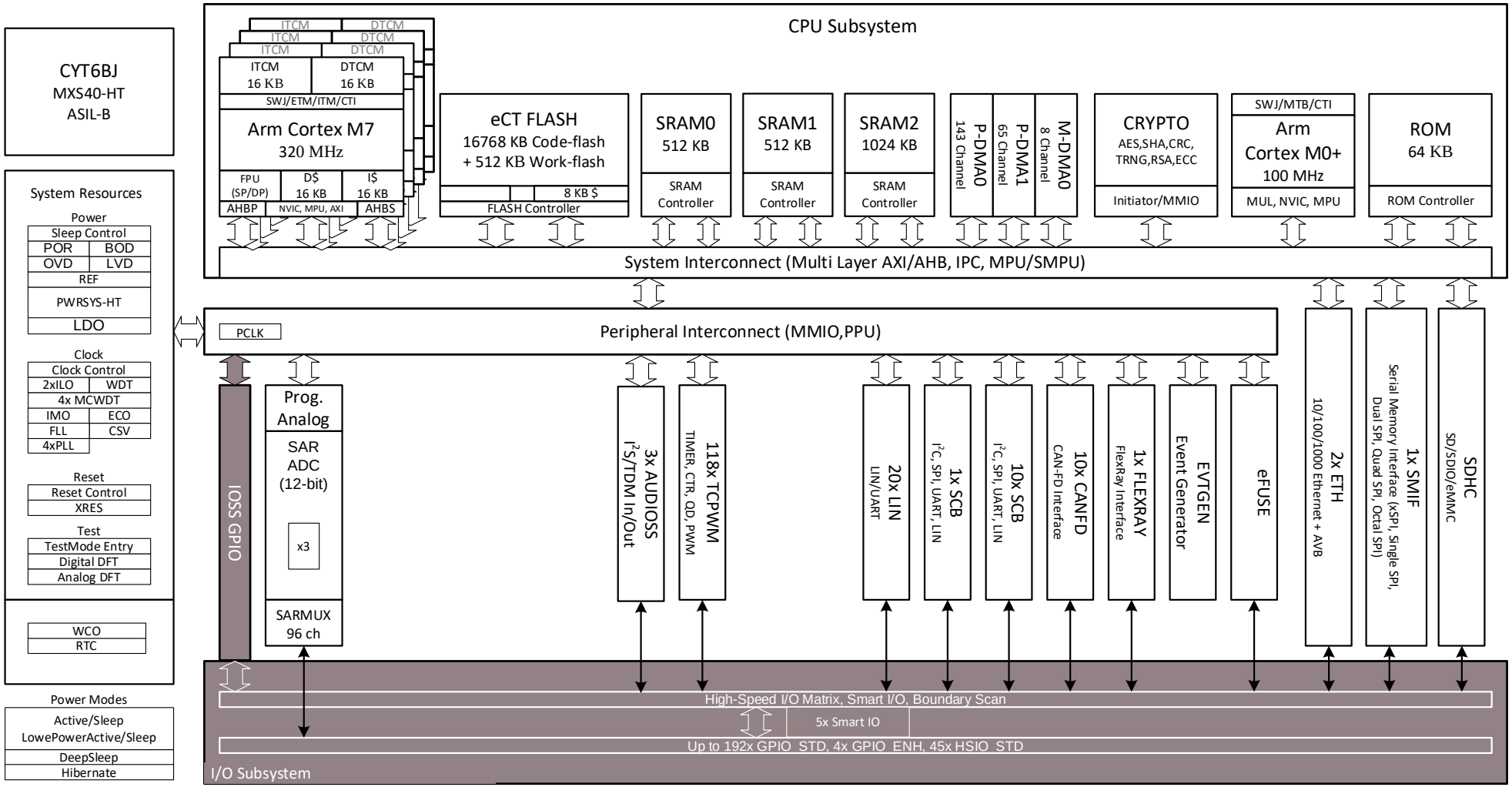


Hint Bar

Training section reference

- **SAR ADC**
- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **CXPI**

CYT6BJ architecture diagram: I/O subsystem



Hint Bar

Training section reference
- I/O Subsystem

TRAVEO™ T2G Cluster Entry

Overview

Features

- Includes Arm® Cortex®-M4 and Cortex®-M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (instrument cluster entry unit, etc.)
- Features
  - LCD controller
    - Up to four LCD controllers, with 32 segments (SEG) and four commons (COM)
    - Supports both Type A (standard) and Type B (low-power) drive waveforms
    - Three drive modes
      - PWM drive at 1/2 bias
      - PWM drive at 1/3 bias
      - Digital correlation
    - Operates in ACTIVE, SLEEP, and DeepSleep power modes
    - Digital contrast control
  - Sound subsystem
    - Two time-division multiplexing (TDM) interfaces
    - Two pulse-code modulation-pulse width modulation (PCM-PWM) interfaces
    - Up to five sound generator (SG) interfaces
    - One PCM audio stream mixer with five input streams

Hint Bar

Review datasheet and TRM chapter 1 for additional details

Overview

Features (continued)

- 32-bit CPU subsystem:
  - CYT2CL: One 160-MHz Cortex®-M4 CPU, with single-cycle multiply, single precision floating point unit (FPU), and memory protection unit (MPU)
  - 100-MHz Cortex®-M0+ CPU with MPU (all devices)
- CYT2CL: Up to 4160 KB of Code Flash along with 128 KB of Work Flash:
  - Dual Bank mode support for Firmware Over-the-Air (FOTA)
- SRAM: CYT2CL: up to 512 KB
- Internal 8-MHz main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
- Power supply rails
  - Internal power supply: VDDD = 2.7 V to 5.5 V
  - 5.0 V I/O for VDDIO_GPIO, VDDIO_SMC = 2.7 V to 5.5 V
  - 3.3 V I/O for VDDIO_HSIO = 3.0 V to 3.6 V
- Hardware Secure Module (HSM) support
- AEC-Q100 qualification and ASIL-B level functional safety

Hint Bar

Review datasheet and TRM chapter 1 for additional details

Overview

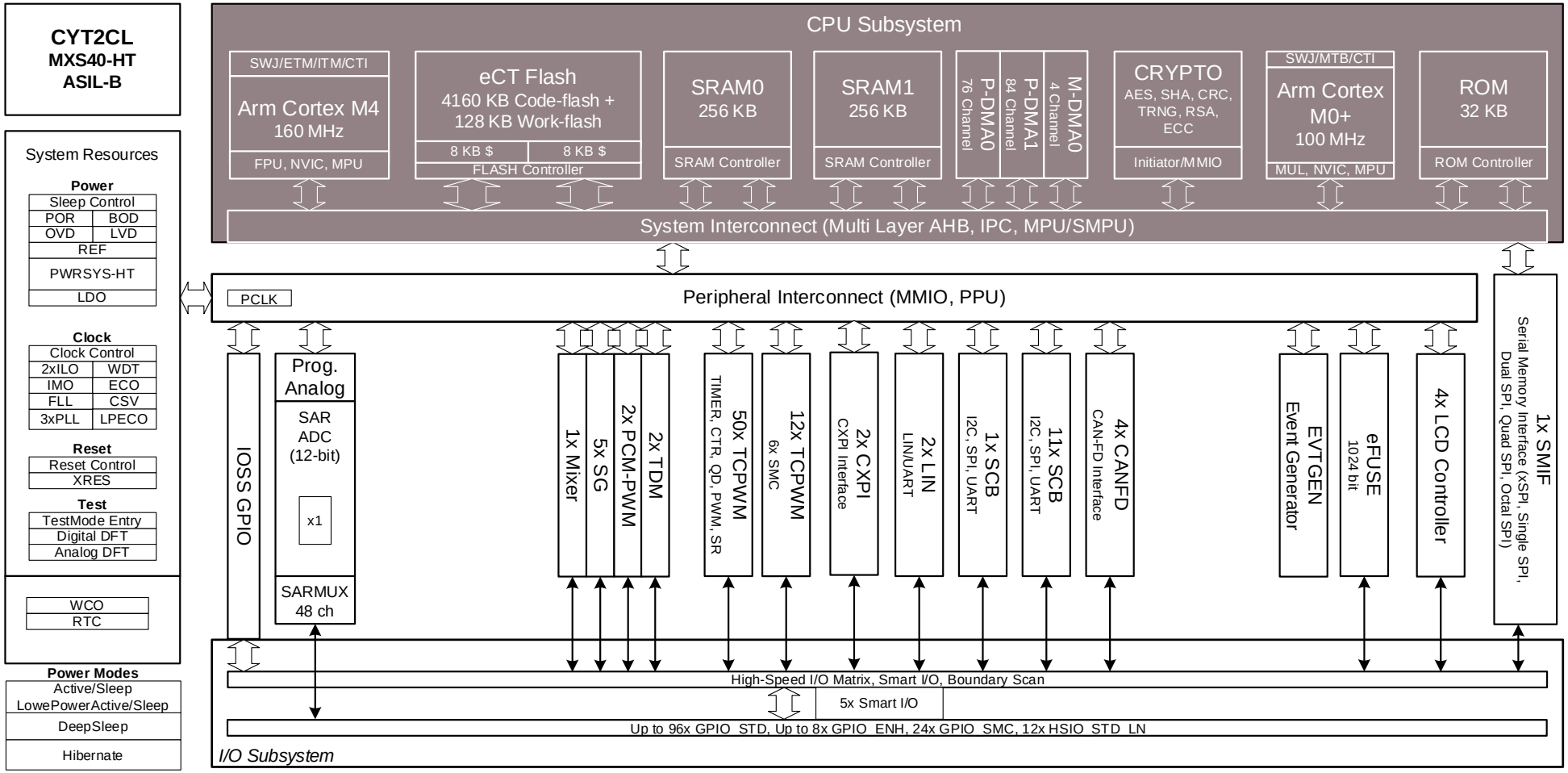
Features (continued)

- Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface
- Packages:
  - CYT2CL: 144-/176-LQFP packages available

Hint Bar

Review datasheet and TRM chapter 1 for additional details

CYT2CL architecture diagram: CPU subsystem



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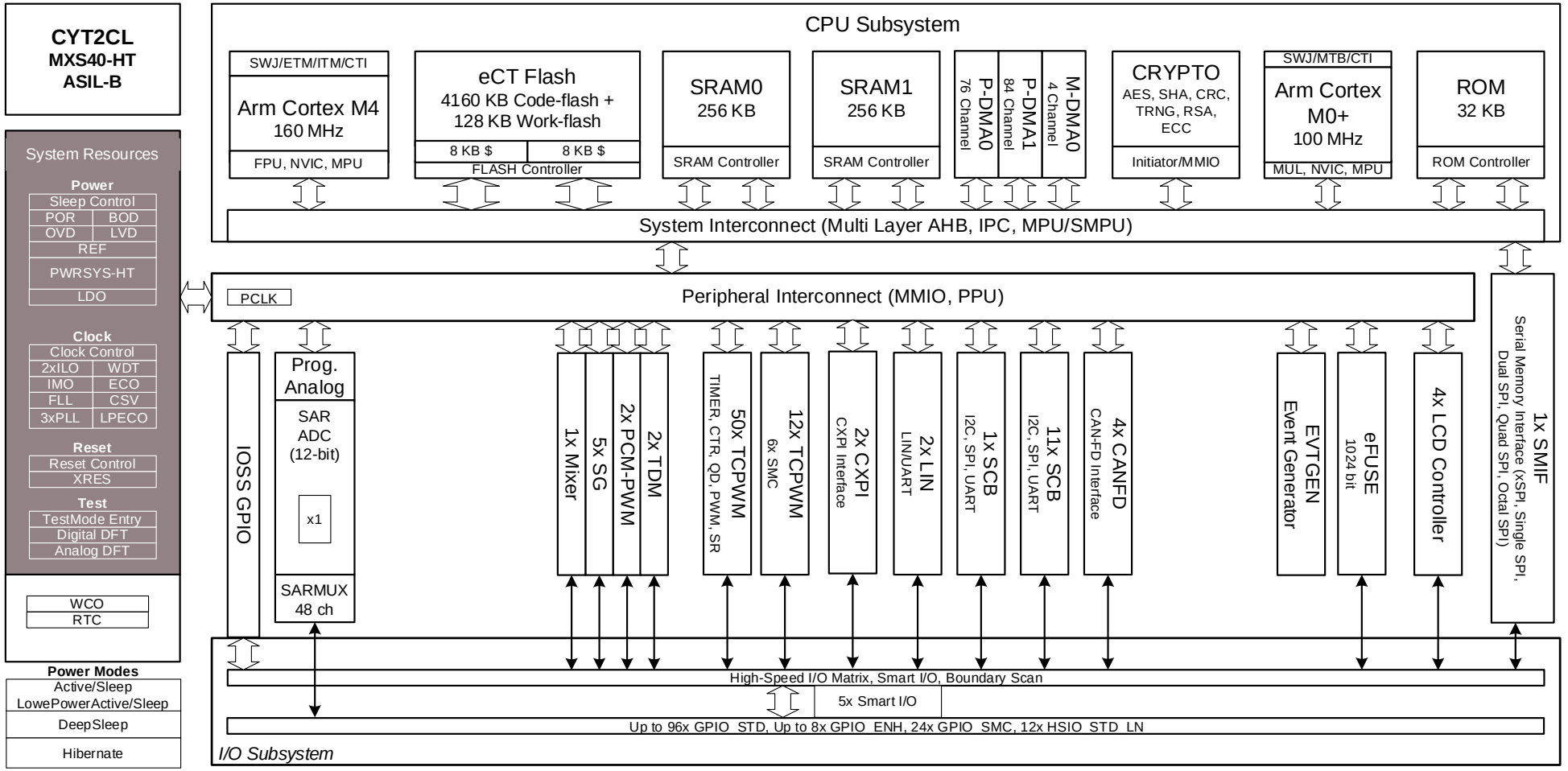
Training section reference

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

CYT2CL architecture diagram: System resources

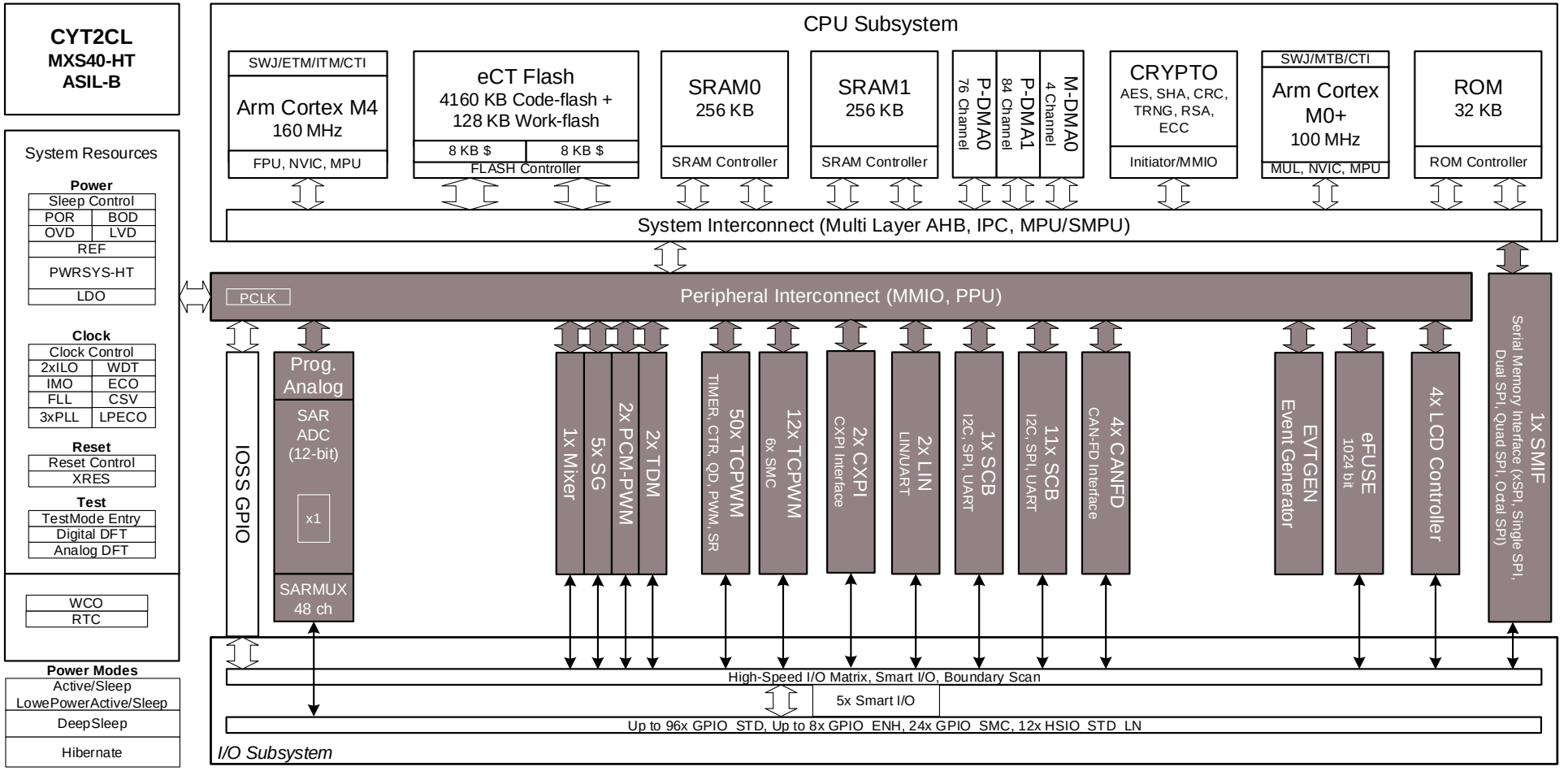


Hint Bar

Training section reference

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

CYT2CL architecture diagram: Peripheral blocks



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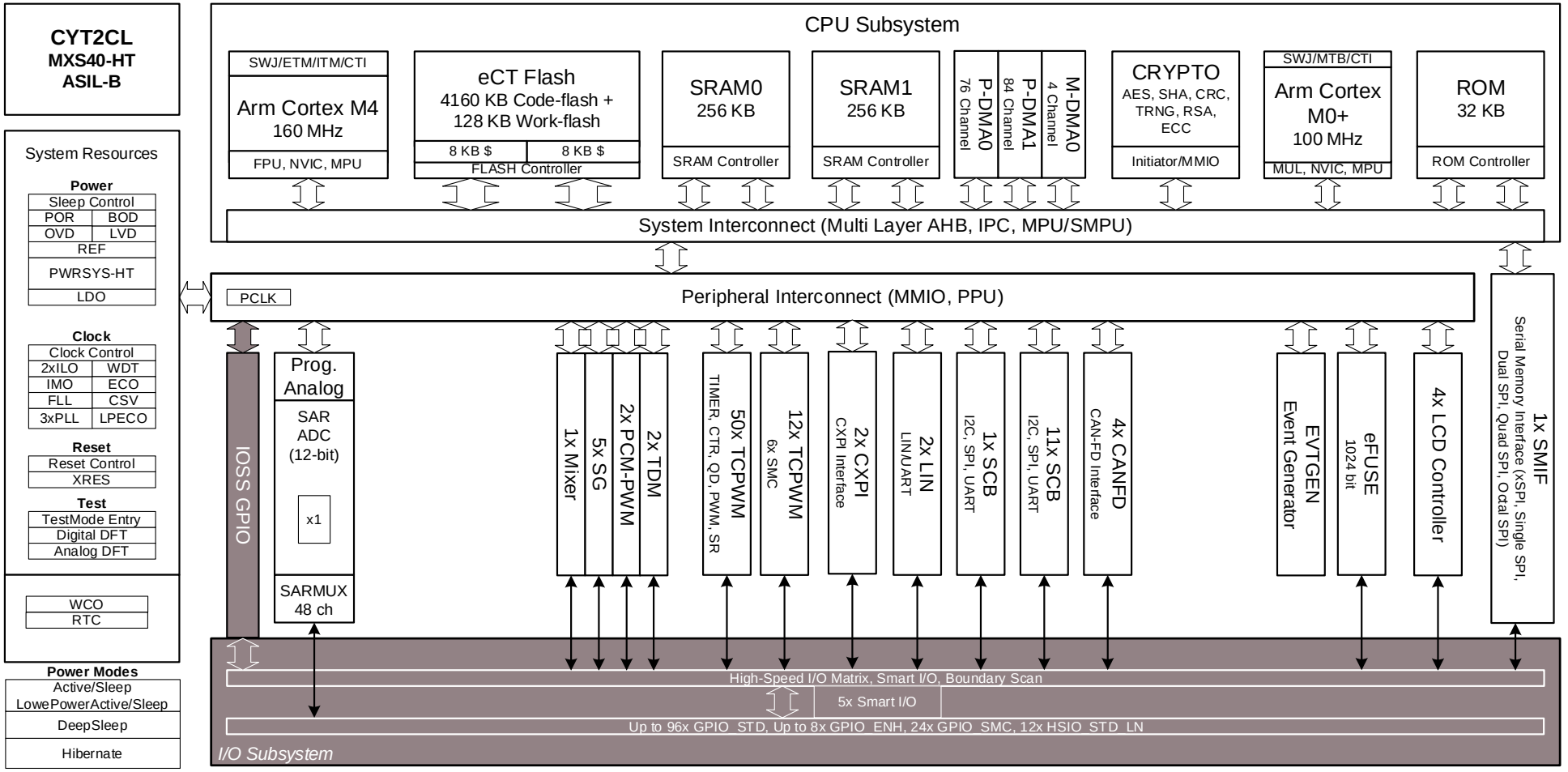
Training section reference

- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **Audio SS**
- **Ethernet**
- **SMIF**
- **Graphics**

CYT2CL architecture diagram: I/O subsystem



Hint Bar

Training section reference

- **I/O Subsystem**
- **SAR ADC**

TRAVEO™ T2G Cluster 2D

Overview

Features

- Includes Arm® dual Cortex®-M7 and Cortex®-M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (instrument clusters, head-up displays, etc.)
- Features
  - Graphics subsystem
    - Supports 2D and 2.5D (perspective warping, 3D effects) graphics rendering
    - Up to 30-bit color resolution (RGB)
    - Embedded video RAM memory (VRAM): CYT3DL: 2048KB, CYT4DN: 4096 KB
    - Up to two video output interfaces supporting two displays
    - One capture engine for video input processing for ITU 656 or parallel RGB/YUV input
  - Sound subsystem

Hint Bar

Review datasheet and TRM chapter 1 for additional details

Overview

Features (continued)

- 32-bit CPU subsystem:
  - CYT3DL: One 240-MHz Cortex®-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
  - CYT4DN: Two 320-MHz Cortex®-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection unit (MPU)
  - 100-MHz Cortex®-M0+ CPU with MPU (all devices)
- CYT3DL: 4160 KB of Code Flash along with 128 KB of Work Flash:
- CYT4DN: 6336 KB of Code Flash along with 128 KB of Work Flash:
  - Dual Bank mode support for Firmware Over-the-Air (FOTA)
- SRAM: CYT3DL: 384 KB, CYT4DN: 640 KB
- Internal 8-MHz main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
- Power supply rails
  - Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  - External (> 300 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD=1.15 V (1.09 V to 1.21 V)
  - 5.0 V I/O for VDDIO_GPIO, VDDIO_SMC = 2.7 V to 5.5 V
  - 3.3 V I/O for VDDIO_HSIO, VDDIO_SMIF_HV = 3.0 V to 3.6 V
  - 1.8 V I/O for VDDIO_SMIF = 1.7 V to 2.0 V
- Hardware Secure Module (HSM) support
- AEC-Q100 qualification and ASIL-B level functional safety

Hint Bar

Review datasheet and TRM chapter 1 for additional details

Overview

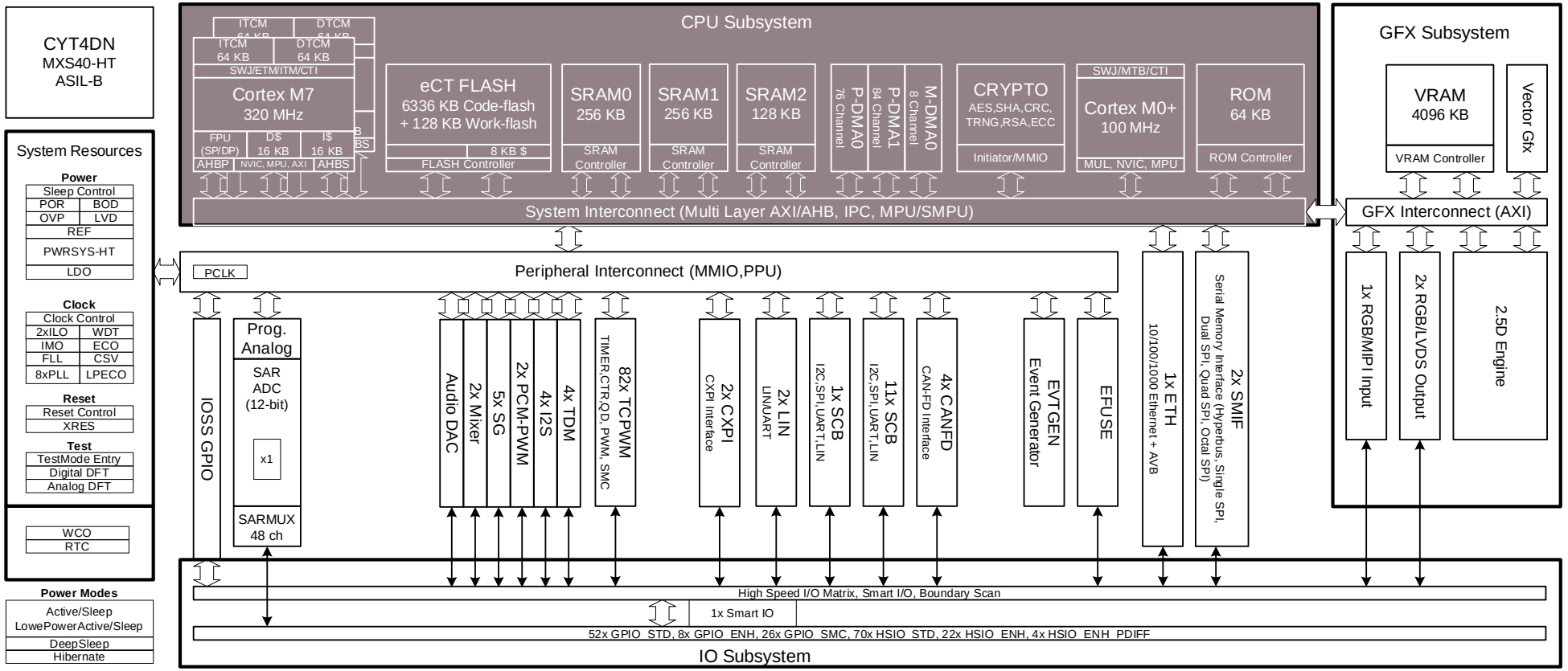
Features (continued)

- Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface
- Packages:
  - CYT3DL: 208-/216-TEQFP, 272-BGA packages available
  - CYT4DN: 327-BGA packages available

Hint Bar

Review datasheet and TRM chapter 1 for additional details

CYT4DN architecture diagram: CPU subsystem

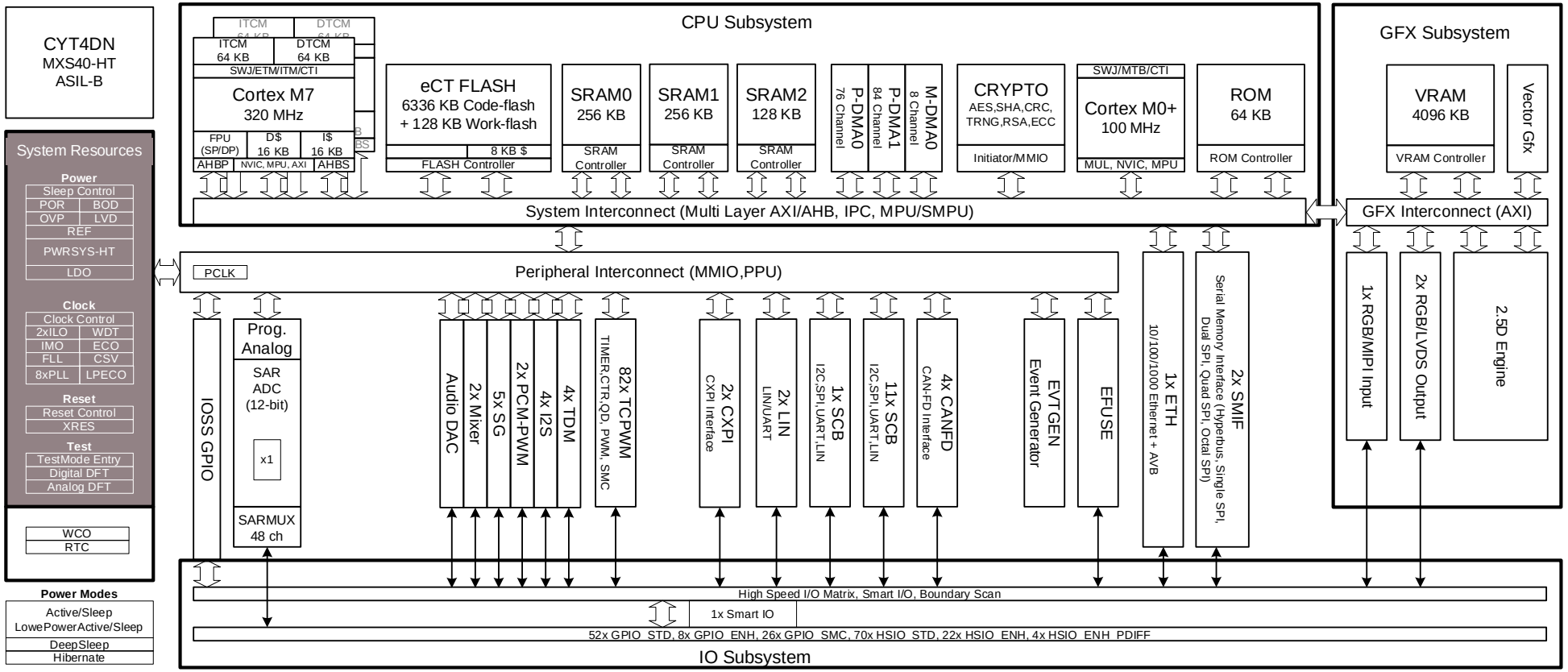


Hint Bar

Training section reference

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

CYT4DN architecture diagram: System resources

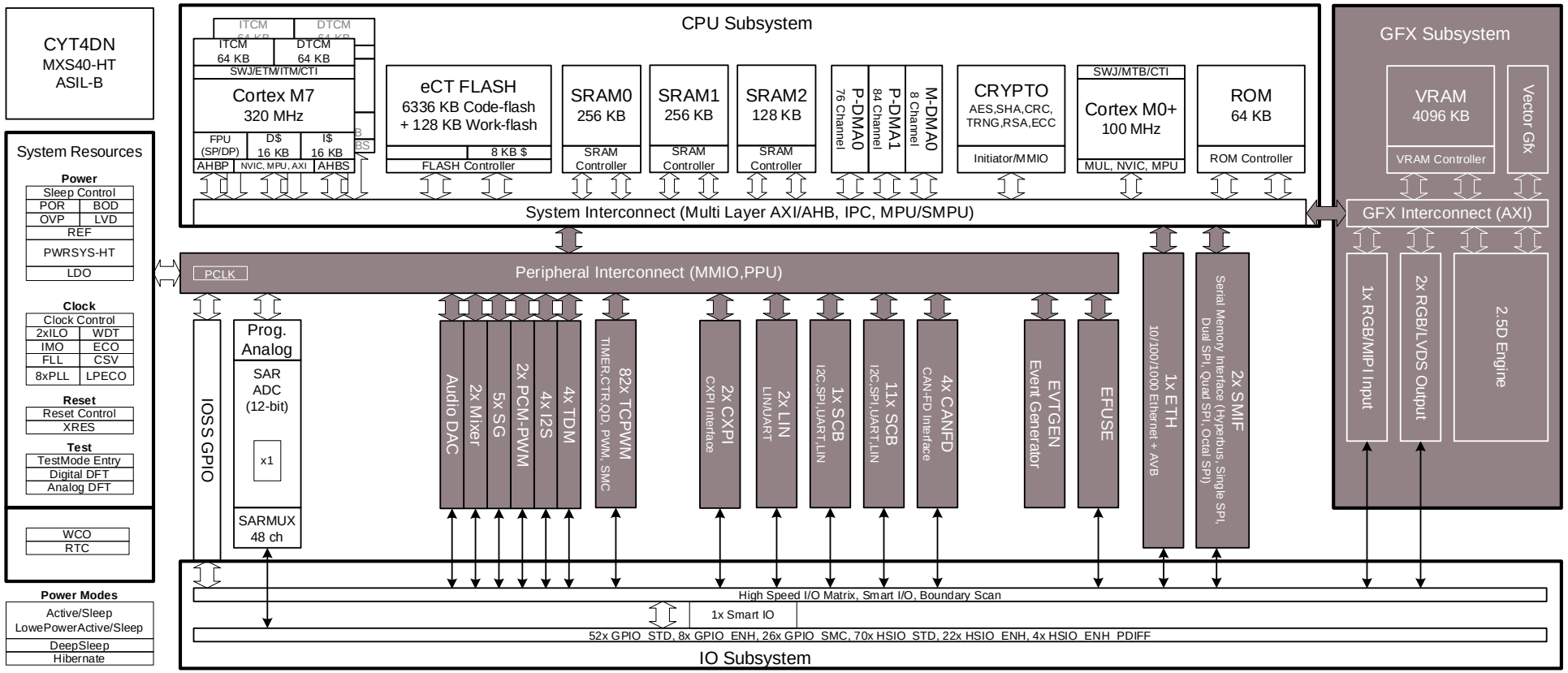


Hint Bar

Training section reference

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

CYT4DN architecture diagram: Peripheral blocks

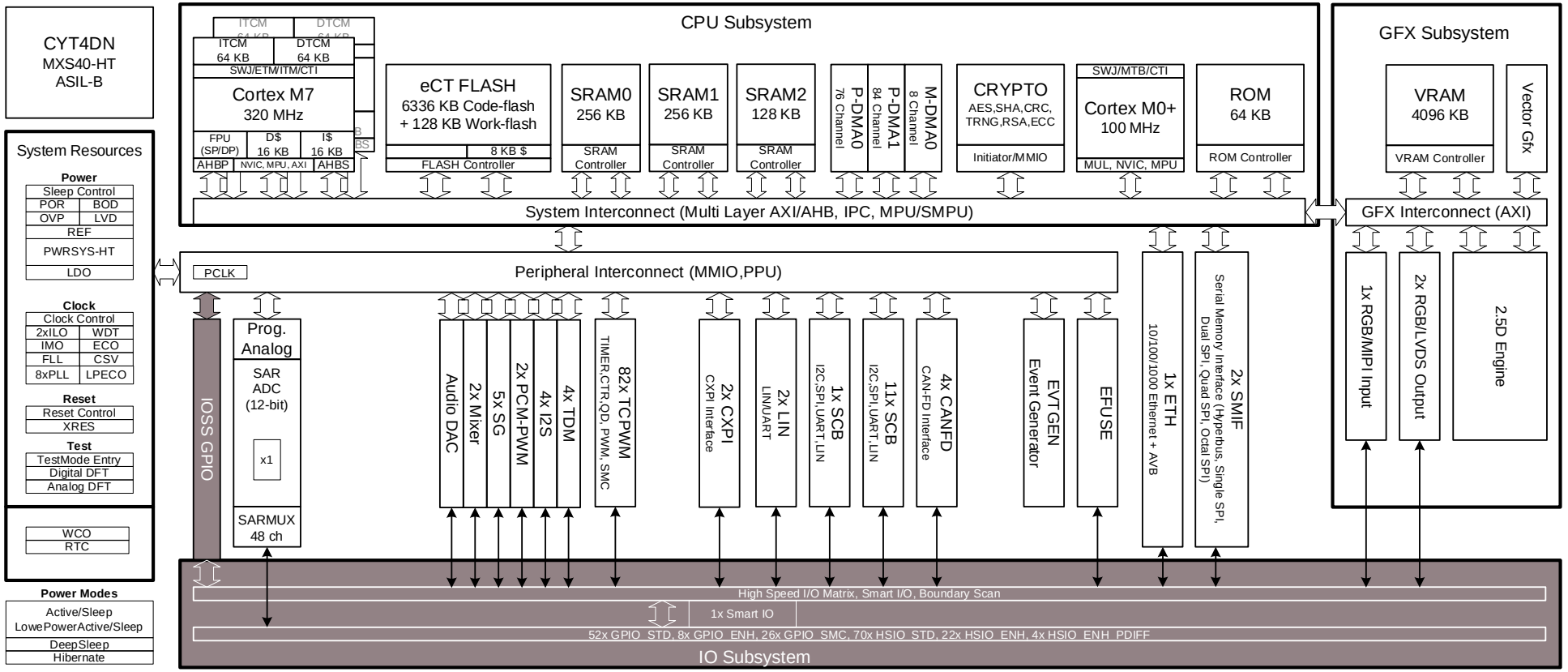


Hint Bar

Training section reference

- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **Audio SS**
- **Ethernet**
- **SMIF**
- **Graphics**

CYT4DN architecture diagram: I/O subsystem



Hint Bar

Training section reference

- **I/O Subsystem**
- **SAR ADC**

Appendix - Comparison between CYT2B, CYT4B, CYT6B, CYT2C, CYT3D, and CYT4D

Feature comparison between CYT2B/CYT4B/CYT6B/CYT2C/CYT3D/CYT4D (1/4)

Features		CYT2B	CYT4B	CYT6B	CYT2C	CYT3D	CYT4D
CPU Subsystem	Main CPU	Cortex-M4 CPU	Two Cortex-M7 CPUs	Four Cortex-M7 CPUs	Cortex-M4 CPU	Cortex-M7 CPU	Two Cortex-M7 CPUs
	FPU	Single-precision	Single/double-precision		Single-precision	Single/double-precision	
	Cache	-	16 KB instruction, 16 KB data		-	16 KB instruction, 16 KB data	
	MPU	Same					
	System Tick Timer	Same					
Inter-Processor Communication (IPC)		Same					
Protection Unit		Same					
Direct Memory Access		Same					
Flash	Bus interface	AHB-Lite	AXI, AHB-Lite		AHB-Lite	AXI, AHB-Lite	
	ECC (SEC/DED)	Same					
	Bank modes	Same					
SRAM Interface	Bus interface	AHB-Lite	AXI, AHB-Lite		AHB-Lite	AXI, AHB-Lite	
	ECC (SEC/DED)	Same					
	TCM	N/A	16 KB ITCM, 16 KB DTCM		N/A	64 KB ITCM, 64 KB DTCM	
Boot		Same					
Interrupts		Same					
Device Security with Crypto		Same					
Chip Operational Modes		Same					
Fault Subsystem		Same					

Feature comparison between CYT2B/CYT4B/CYT2C/CYT3D/CYT4D (2/4)

Features		CYT2B	CYT4B	CYT6BJ	CYT2C	CYT3D	CYT4D
Power Supply and Monitoring	Power supply	V_{DDD} = 2.7 V to 5.5 V	V_{DDD} = 2.7 V to 5.5 V (up to 300 mA) V_{DDD} = 2.7 V to 5.5 V and V_{CCD} = 1.15 V (exceeds 300 mA)		V_{DDD} = 2.7 V to 5.5 V	V_{DDD} = 2.7 V to 5.5 V (up to 300 mA) V_{DDD} = 2.7 V to 5.5 V and V_{CCD} = 1.15 V (exceeds 300 mA)	
	5.0 V I/O power supply	V_{DDIO_1}, V_{DDIO_2}			V_{DDIO_GPIO}, V_{DDIO_SMC}		
	3.3 V I/O power supply	N/A	V_{DDIO_3}, V_{DDIO_4}		V_{DDIO_HSIO}	V_{DDIO_HSIO}, $V_{DDIO\_SMIF\_HV}$	
	1.8 V I/O power supply	N/A				V_{DDIO_SMIF}	
	Analog power supply	V_{DDA}				V_{DDA_ADC}, V_{DDA_DAC}, V_{DDA_MIPI}, V_{DDA_FPDx}, V_{DDHA_FPDx}, V_{DDPLL_FPDx},	
	Active/DeepSleep regulator	Same					
	External transistor control	N/A	Available	N/A	N/A		
	External PMIC control	N/A	Available		N/A	Available	
	BOD/OVD/LVD	Same					
Device Power Modes		Same					
Clock System	Internal clock sources (IMO, ILO)	Same					
	External clock sources (ECO, WCO, EXT_CLK)	Same				Support LPECO	
	FLL	Same					
	PLL without SSCG and fractional operation	Same					
	PLL with SSCG and fractional operation	N/A	Available				
	Clock supervision (CSV)	Same					
	Clock calibration counter	Same					
Reset System		Same					

Feature comparison between CYT2B/CYT4B/CYT2C/CYT3D/CYT4D (3/4)

Features		CYT2B	CYT4B	CYT6BJ	CYT2C	CYT3D	CYT4D
Watchdog Timer		Same					
Real Time Clock		Same					
I/O System	GPIO input modes (CMOS/TTL/Automotive)	Same					
	Eight output drive modes	Same					
	Drive strength (Full, 1/2, 1/4)	Same					
	Slew rate control (only for GPIO_ENH)	Same					
	GPIO interrupt	Same					
	Smart I/O	Same					
	GPIO SMC	N/A	N/A		Available		
	High-speed I/O	N/A	Available (HSIO_STD)		N/A	Available (HSIO_STD, HSIO_ENH, HSIO_ENH_PDIFF)	
CAN FD		Same					
Serial Communications Block		Same					
TCPWM		Same					
LIN		Same					
Event Generator		Same					
Trigger Multiplexer		Same					
FlexRay		N/A	Available		N/A		
Ethernet MAC		N/A	Available		N/A	Available (N0 GMII)	

Feature comparison between CYT2B/CYT4B/CYT2C/CYT3D/CYT4D (4/4)

Features	CYT2B	CYT4B	CYT6BJ	CYT2C	CYT3D	CYT4D
LCD Controller	N/A			Available	N/A	
Serial Memory Interface	N/A	Available (100 MHz)		Available (100 MHz)	Available (100 MHz: TEQFP/ 133 MHz: BGA package)	Available (200 MHz)
SDHC Host Controller	N/A	Available		N/A		
Audio Subsystem (I^2S/TDM)	N/A	Available		N/A		
Sound Subsystem (I^2S/TDM/Audio DAC/Mixer/PWM/Sound Generator)	N/A			Available		
Graphics Subsystem	N/A			N/A	Available	
SAR ADC	Same					
Program and Debug Interface	Same					
Nonvolatile Memory Programming	Same					

Revision history

Revision	ECN	Submission Date	Description of Change
**	6097587	09/03/2018	Initial release
*A	6401071	12/04/2018	Added CYT2B9 and CYT4BF Updated the Block Diagram
*B	6682714	09/26/2019	Updated title to include cluster Removed page 3 Updated CM0+ frequency from 80 MHz to 100 MHz Added CYT4DN (page 17 to 23, 34 to 38) Updated Functional Overview in Appendix
*C	7053676	12/24/2020	Updated page 2, 5 to 10, 12, 13, 19, 20, 21
*D	7486165	11/30/2021	Added CYT2CL Updated and optimized for all pages
*E	8016625	03/25/2024	Added CYT6BJ