MCMCAN
CAN Interface

AURIX™ TC3xx Microcontroller Training
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MCMCAN
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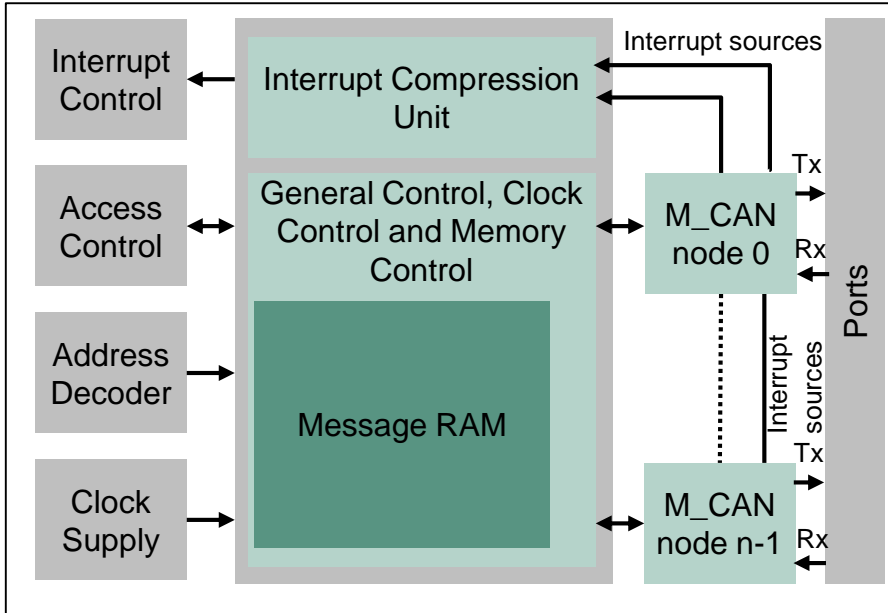
Highlights

AURIX™ TC3xx MCMCAN module conforms to the ISO 11898-1 (including CAN FD) and ISO 11898-4 (TTCAN), therefore event synchronized time-triggered communication, global system time and clock drift compensation are provided.

Up to 8 Mbit/s data transfer rate for CAN FD, programmable for each node.

Key Features

Configurable Message RAM
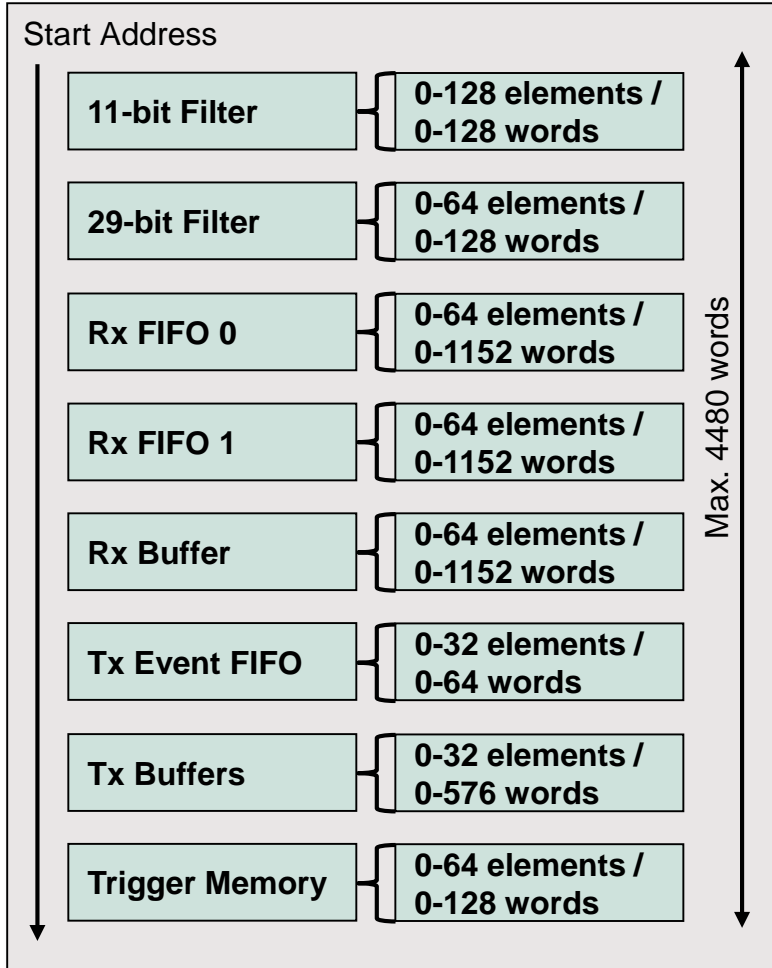
Up to 4 independent CAN nodes

Configurable transmit and receive FIFOs

Customer Benefits

Easy setup of the required memory for each node

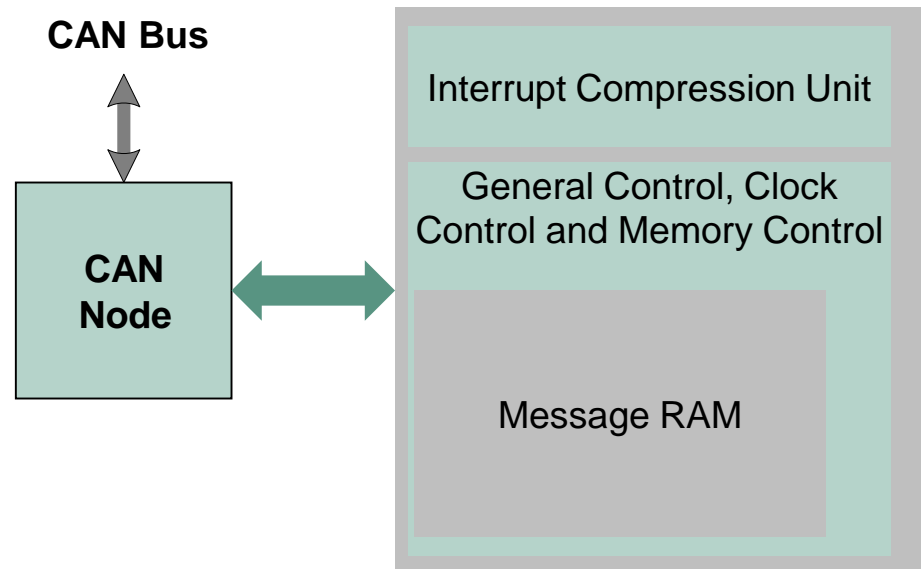Dedicated control registers for each CAN node increasing system flexibility

Each FIFO can be resized to meet the requirements of the application

MCMCAN
Configurable Message RAM

Start Address

11-bit Filter	0-128 elements / 0-128 words

29-bit Filter	0-64 elements / 0-128 words

Rx FIFO 0	0-64 elements / 0-1152 words

Rx FIFO 1	0-64 elements / 0-1152 words

Rx Buffer	0-64 elements / 0-1152 words

Tx Event FIFO	0-32 elements / 0-64 words

Tx Buffers	0-32 elements / 0-576 words

Trigger Memory	0-64 elements / 0-128 words

Max. 4480 words

› The Message RAM is shared across all CAN nodes

› The RAM structure is defined via the start address of different element blocks

› The size of each element can be individually configured, therefore the total memory defined for message RAM depends on the byte sizes of each element

› It is not necessary to configure each of the sections and there are no restrictions with respect to the order of the element blocks
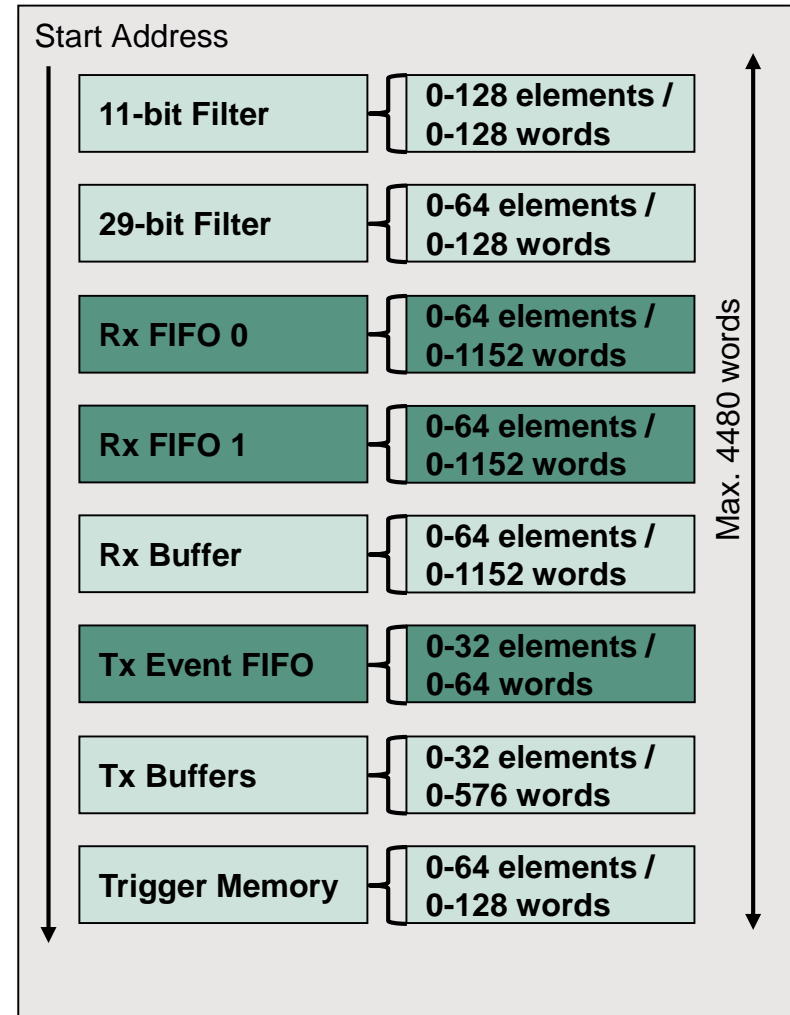
› Strong filtering capabilities

MCMCAN
Up to 4 independent CAN nodes

› Up to 4 independent CAN nodes flexibly connected to the Message RAM:

- Baud rate settings

- Operation and events control

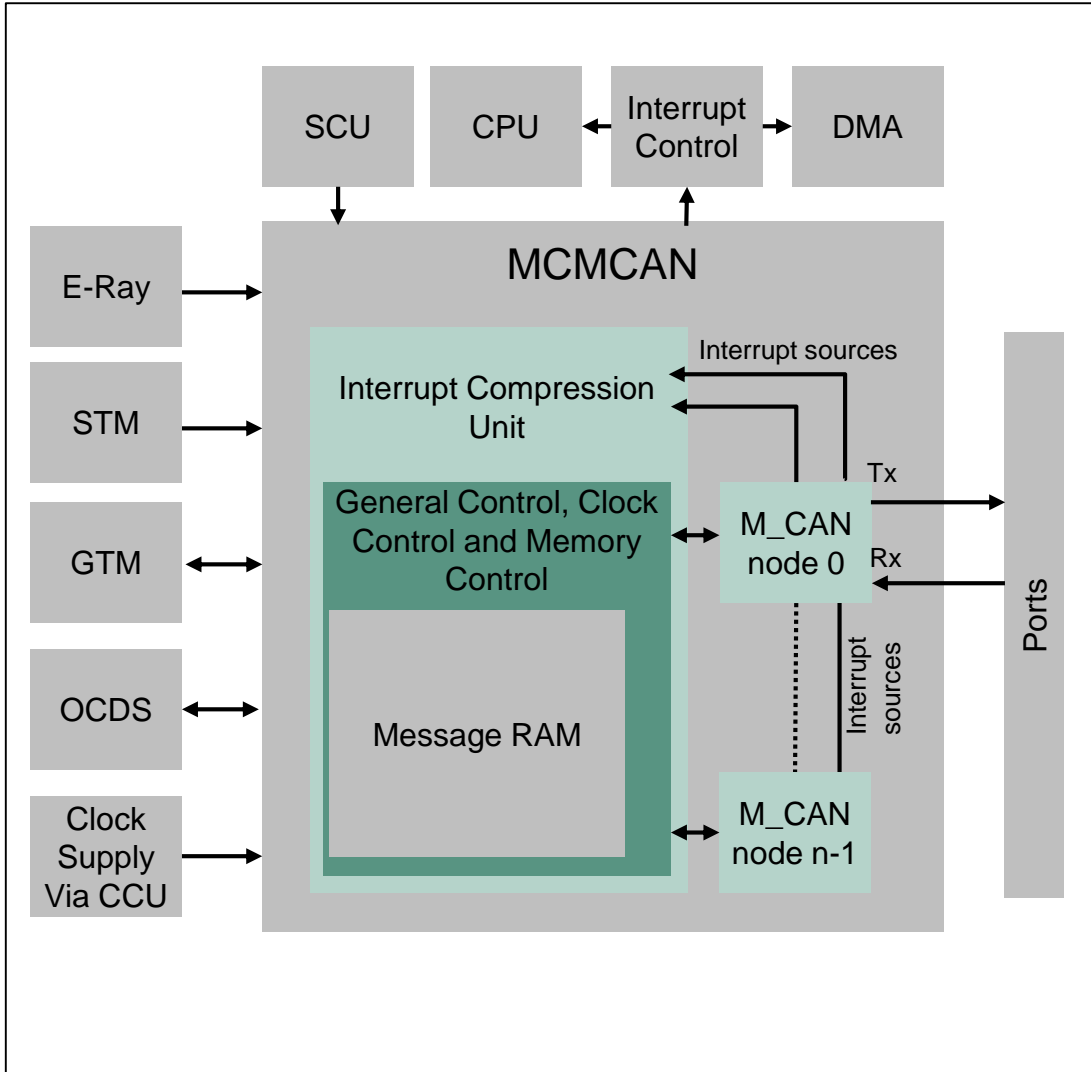- Ports control

- Error analysis

- Timer Event

CAN Bus

CAN Node

Interrupt Compression Unit

General Control, Clock Control and Memory Control

Message RAM

MCMCAN
Configurable transmit and receive FIFOs

› Rx FIFO 0 and RX FIFO 1 can be configured to hold up to 64 elements each

› In order to avoid an Rx FIFO overflow, the Rx FIFO watermark can be used. When the fill level reaches the watermark, an interrupt flag is set

› Tx FIFO can be configured to hold up to 32 elements

› The messages stored in the Tx FIFO are transmitted based on an index, which is incremented cyclically until the Tx FIFO is empty

› The Tx FIFO enables the transmission of messages with the same Message ID from different Tx Buffers in the order they were written to the Tx FIFO

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MCMCAN
System integration

System integration

Each Transmit/Receive line of every CAN node is available for several external ports through the port control logic.

Up to 16 interrupt lines connect ICU for CPU trigger and DMA service or as signal trigger of the GTM action.

Debugging of the MCMCAN module can be done using the trigger lines connected to OCDS.

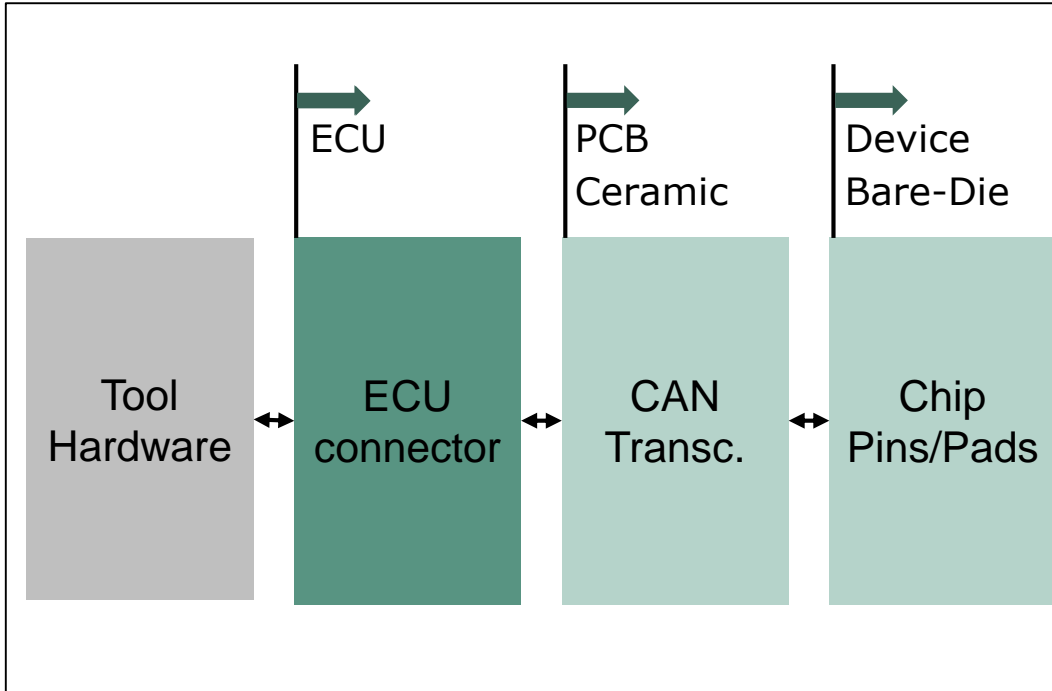## Target applications

Automotive/Motor control

Industrial automation

Connectivity

General purpose

Application example
Debugging via CAN

Overview

There are two tool interfaces that are using MCMCAN:

› DAP over CAN Physical Layer (DXCPL)

› DAP over CAN Messages (DXCM)

The main use case for DXCPL is the analysis of field returns. DXCPL is using DAP telegrams wrapped in CAN messages. Once DXCPL is activated, the CAN node is disconnected from the CAN bus.

In the case that the CAN node cannot be dedicated only for debugging, DXCM is sharing the bandwidth with the CAN node. In the case of DXCM, debug messages are sent together with the CAN node messages.

Advantages

The CAN bus signals are usually available at the ECU connector, therefore this physical connection allows to use of different types of tools without opening the ECU housing.

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